SOC Octal High Density PPMU

The Mt. Hood is a highly integrated System-on-a-Chip (SoC) High Density PPMU solution incorporating 8 independent channels of PPMU. The interface and control are digital. All analog circuitry is inside the chip. Eight complete and independent channels are integrated into each chip. For most tester applications, no additional analog hardware needs to be developed or used on a per-pin basis.

Features

- Per-Pin PMU
  - FV, FI, MV, MI
  - 4 Quadrant Operation
  - –2V to 6.5V FV/MV Range
  - 6 Current Ranges (±2µA, ±20µA, ±200µA, ±2mA, ±15mA, ±50mA)
  - Programmable Voltage and Current Clamps
  - Resistive Load Function (12 Selectable Resistor Values)
  - Reduced Glitch Current Range Changing
- Protection
  - On-Chip Junction Temperature Monitor
- Global FORCE/SENSE Connectable to any Channel
- Remote Sense from Adjacent Channel
- 100MHz SPI Interface
- On-Chip Independent DACs to Generate DC Levels
  - 6 DC Levels per Channel
    - 2x 16-bit for Forcing Function
    - 2x 8-bit for Clamps
    - 2x 4-bit for Current Clamps
    - On-Chip Offset and Gain Correction
- Power Management
  - Independent Output Buffer Power Supply for both positive and negative currents to minimize power (VCCO and VEEO)
- Monitor
  - Two MV/MI Monitors (one for each 4 channels)
  - Ability to Route any Channel to Either Monitor
  - On-Chip Signal Preconditioning (Optimized for Direct Connection to AD7609B)
- Package/Power Dissipation
  - 88 Pad, 10mm x 10mm MLF
  - Pdq 150mW/Channel
  - Pstandby 75mW/Channel

Applications

- Automated Test Equipment
- Instrumentation

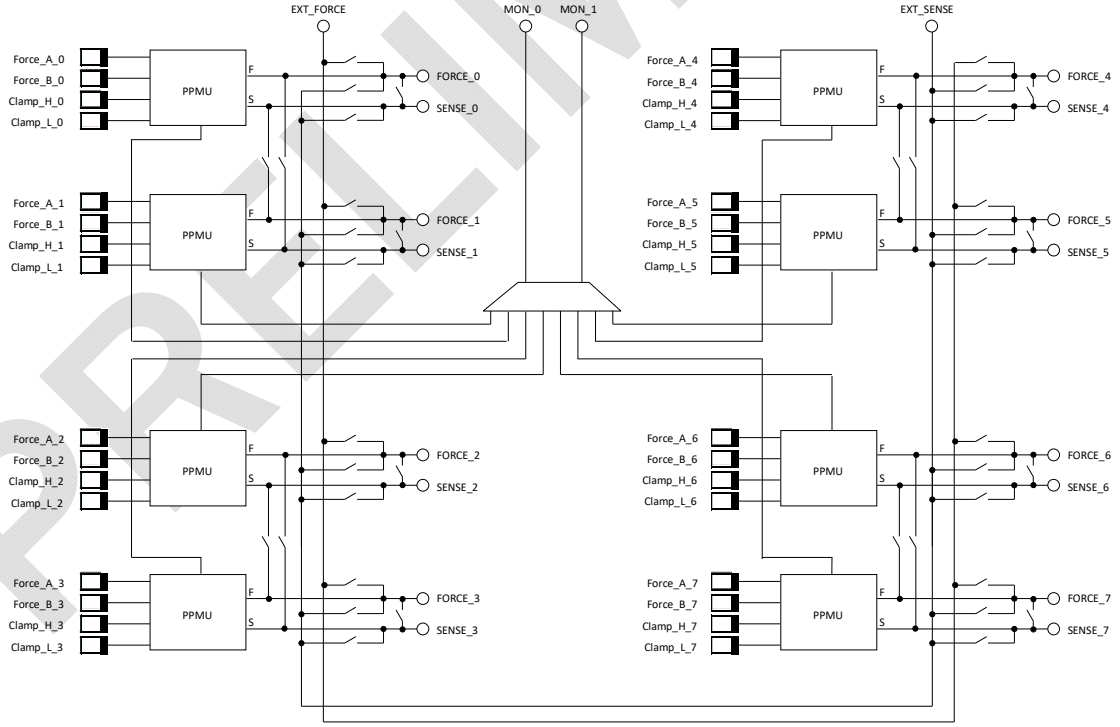

Table of Contents

Table of Tables

Table of Figures

Pin Descriptions

TABLE 1: PIN DESCRIPTIONS

PIN #	PIN NAME	DESCRIPTION
Power Supplies		
2, 7, 14, 19, 46, 51, 58, 63	VCCO	High Current Supply.
4, 9, 16, 21, 28, 33, 41, 48, 53, 60, 65	VCC	Positive voltage supply.
24, 27, 31, 38, 44, 67, 88	VEE	Negative voltage supply.
1, 6, 13, 18, 45, 50, 57, 62	VEEO	Negative Current Supply
23	VHH	High voltage digital supply.
12, 55, 74, 82, 84	GND	Ground supply.
34, 36, 75	GNDA	Analog Ground supply.
70, 72	GND_IO	IO Ground supply.
11, 56, 81	VDD	Digital block and logic supply.
35, 37, 78	VDDA	Analog supply. Clean VDD primarily used for DACs.
83, 71	VDD_IO_IN, VDD_IO_OUT	Analog Supply. Used for SPI IO.
Analog Pins		
25	EXT_SENSE	Measure high DC calibration bus, unbuffered.
26	EXTSENSE_REF	Measure low DC calibration bus, unbuffered.
29	EXT_FORCE	Force high DC calibration bus.
42, 39	MON[1:0]	ADC measure high odd [1] and even [0] channels.
43, 40	MON_REF[1:0]	ADC measure low odd [1] and even [0] channels.
64, 59, 52, 47, 3, 8, 15, 20	FORCE[7:0]	Force outputs.
66, 61, 54, 49, 5, 10, 17, 22	SENSE[7:0]	Sense inputs.
30	GND_REF	Analog reference ground (no current, sense only).
32	DGS	DUT ground reference.
77	VREF	Precision analog reference voltage.
76	RREF	Connect an external precision reference resistor to GND.
SPI Interface		
85	SPI_CLK	SPI serial bus clock input. 50Ω terminated to VDD/2.
86	SPI_SDI_A	SPI serial data input. 50Ω terminated to VDD/2.
80	SPI_SDI_B	SPI serial data input. 50Ω terminated to VDD/2.
73	SPI_SDO_A	SPI serial data input. 50Ω terminated to VDD/2.
69	SPI_SDO_B	SPI serial data input. 50Ω terminated to VDD/2.
87	SPI_CS	SPI chip select input. Functions as SCAN enable input when TESTEN is high. 50Ω terminated to VDD/2.
79	RESET	Full chip rEset input. Active high. Pulled up on chip through 50kΩ to VDD.
61	SCAN_ENA	

Pin Configuration

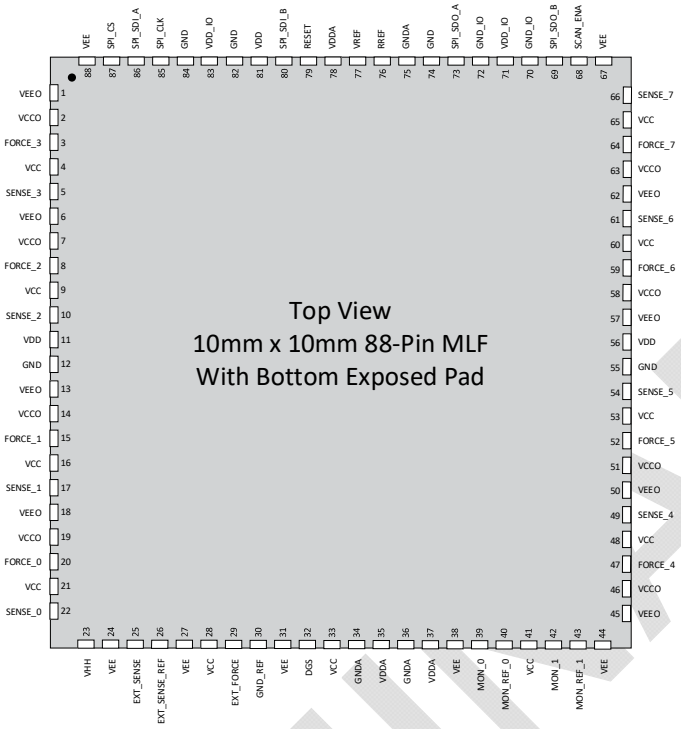

FIGURE 1: PIN CONFIGURATION TOP VIEW

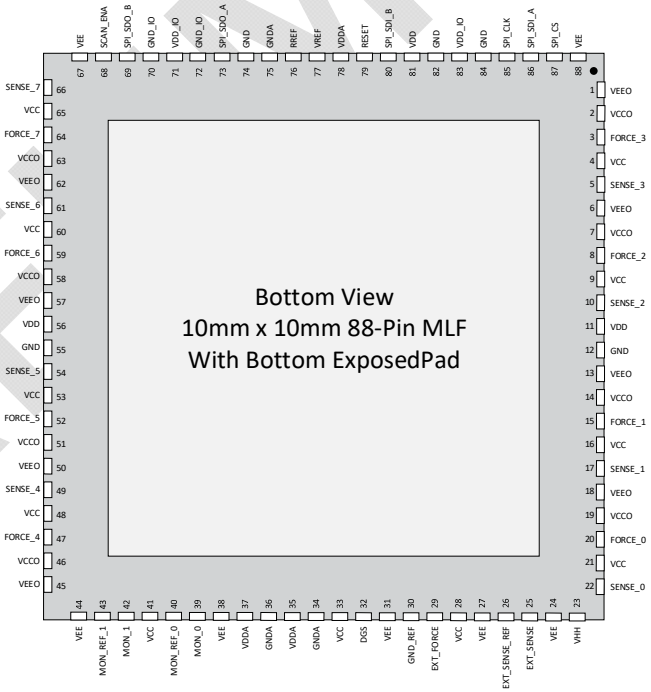

FIGURE 2: PIN CONFIGURATION BOTTOM VIEW

Absolute Maximum Ratings

TABLE 2: ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies					
Positive Analog Supply Voltage	V_{CC_ABS}	–0.5	7.5	8	V
Positive Analog Supply Voltage	V_{HH_ABS}	–0.5	15	16	V
Positive Driver Supply Voltage	V_{CCO_ABS}	–0.5	5.5	6	V
Digital Supply Voltage/Analog Supply Voltage	V_{DD}/V_{DDA_ABS}	–0.5	1.8	1.98	V
Negative Analog Supply Voltage	V_{EE_ABS}	–4.0	–3.5	0.5	V
Negative Driver Supply Voltage	V_{EEO_ABS}	–2.0	–1.5	0.5	V
Total Analog Supply [VCC-VEE]	$V_{DIF\_CE\_ABS}$	–0.5	11	11.5	V
Total Analog Supply [VHH-VEE]	$V_{DIF\_HE\_ABS}$	–0.5	18.5	20	V
Total Driver Supply Voltage [VCC-VEEO]	$V_{DIF\_OUT\_ABS}$	–0.5	7	7.5	V
PPMU					
Force Voltage Output/Measure Voltage Input Range/Voltage Clamp Range	$V_{RNG\_FRC\_ABS}$	VEE		VCC	V
Force Current/Measure Current Range					
IR0 – Range 0	$I_{RNG\_FORCE0\_ABS}$	–3		3	µA
IR1 – Range 1	$I_{RNG\_FORCE1\_ABS}$	–30		30	µA
IR2 – Range 2	$I_{RNG\_FORCE2\_ABS}$	–300		300	µA
IR3 – Range 3	$I_{RNG\_FORCE3\_ABS}$	–3		3	mA
IR4 – Range 4	$I_{RNG\_FORCE4\_ABS}$	–55		55	mA
Force Current/Measure Current Compliance Range	$V_{RNG\_CMPL\_ABS}$	See Figure ??			V
CVA_PPMU – Go-no-Go Comparator Threshold “A”	$V_{RNG\_PMUCVA\_ABS}$	–2.1		6.1	V
CVB_PPMU – Go-no-Go Comparator Threshold “B”	$V_{RNG\_PMUCVB\_ABS}$	–2.1		6.1	V
External References					
Reference Voltage (VREF to VGND_REF)	$V_{RNG\_REF\_ABS}$	–0.5	1.25	1.8	V
GND_REF Voltage Range (relative to GND)	$V_{RNG\_GNDREF\_ABS}$	–0.5		0.5	V
RREF – External Reference Resistor Value	$R_{RNG\_RREF\_ABS}$	–1%	12.4	+1%	kΩ
DGS Voltage Range (Relative to GND)	$V_{RNG\_DGS\_ABS}$	–500		500	mV
EXT_FRC – External Force Voltage Range	$V_{RNG\_EXTFRC\_ABS}$	VEE – 0.5		VCC + 0.5	V
EXT_SNS – External Sense Voltage Range	$V_{RNG\_SNSLO\_ABS}$ $V_{RNG\_SNSHI\_ABS}$	VEE – 0.5		VCC + 0.5	V
Miscellaneous					
Maximum Junction Temperature Range	T_{JUNC_ABS}	0		125	°C

Recommended Operating Conditions

TABLE 3: RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies					
Positive Analog Supply Voltage	V_{CC}	7.27	7.5	7.72	V
Positive Analog Supply Voltage	V_{HH}	14.55	15	15.45	V
Positive Driver Supply Voltage	V_{CCO}	5.34	5.5	5.66	V
Digital Supply Voltage/Analog Supply Voltage	V_{DD}/V_{DDA}	1.75	1.8	1.85	V
Negative Analog Supply Voltage	V_{EE}	–3.6	–3.5	–3.4	V
Negative Driver Supply Voltage	V_{EEO}	–1.55	–1.5	–1.46	V
Total Analog Supply |VCC – VEE|	V_{DIF_CE}	10.67	11	11.33	V
Total Analog Supply [VHH – VEE]	V_{DIF_HE}	17.95	18.5	19.06	V
Total Driver Supply [VCCO – VEEO]	V_{DIF_OUT}	6.79	7	7.21	V
PPMU					
Force Voltage Output/Measure Voltage Input Range/Voltage Clamp Range	V_{RNG_FRC}	–2		6	V
Force Current/Measure Current Range					
IR0 – Range 0	I_{RNG_FORCE0}	–2		2	µA
IR1 – Range 1	I_{RNG_FORCE1}	–20		20	µA
IR2 – Range 2	I_{RNG_FORCE2}	–200		200	µA
IR3 – Range 3	I_{RNG_FORCE3}	–2		2	mA
IR4 – Range 4	I_{RNG_FORCE4}	–50		50	mA
Force Current/Measure Current Compliance Range	V_{RNG_CMPL}	See Figure 29			V
CVA_PPMU – Go-no-Go Comparator Threshold “A”	V_{RNG_PMUCVA}	–2		6	V
CVB_PPMU – Go-no-Go Comparator Threshold “B”	V_{RNG_PMUCVB}	–2		6	V
External References					
Reference Voltage (VREF– VGG_REF)	V_{RNG_REF}	1.2375	1.25	1.2625	V
GND_REF – Voltage Range (relative to GND)	V_{RNG_GNDREF}	–50		50	mV
RREF – External Reference Resistor Value	R_{RNG_REXT}	12.276	12.4	12.524	kΩ
DGS Voltage Range (Relative to GND)	V_{RNG_DGS}	–300		300	mV
EXT_FRC – External Force Voltage Range	V_{RNG_EXTFRC}	VEE		VCC	V
EXT_SNS_LO, EXT_SNS_HI - External Sense Voltage Range	V_{RNG_SNSLO} V_{RNG_SNSHI}	VEE		VCC	V
Miscellaneous					
Junction Operating Temperature Range	T_{JUNC}	25		100	°C

DC Characteristics

NOTE: For all of the following DC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DC Electrical Specifications – Power Supplies

V_{DGS}=0V for all tests

TABLE 4: DC ELECTRICAL SPECIFICATIONS - POWER SUPPLIES

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
POWER Setup A: POR (Power On Reset) Note 1							
	VCC Current Setup A		I_{CC_A}				mA
	VHH Current Setup A		I_{HH_A}				mA
	VCCO Current Setup A		I_{CCO_A}				mA
	VDD/A Current Setup A		I_{DD_A}				mA
	VEE Current Setup A		I_{EE_A}				mA
	VEEO Current Setup A		I_{EEO_A}				mA
POWER Setup B: PMUFV (PMU Force Voltage Open) Note 1							
	VCC Current Setup B		I_{CC_B}				mA
	VHH Current Setup B		I_{HH_B}				mA
	VCCO Current Setup B		I_{CCO_B}				mA
	VDD/A Current Setup B		I_{DD_B}				mA
	VEE Current Setup B		I_{EE_B}				mA
	VEEO Current Setup B		I_{EEO_B}				mA
POWER Setup C: HSDRIVE (High Speed Driver with Deskew) Note 1							
	VCC Quiescent Current Setup C		$I_{CC\_C\_Q}$				mA
	VHH Quiescent Current Setup C		$I_{HH\_C\_Q}$				mA
	VCCO Quiescent Current Setup C		$I_{CCO\_C\_Q}$				mA
	VDD/A Quiescent Current Setup C		$I_{DD\_C\_Q}$				mA
	VEE Quiescent Current Setup C		$I_{EE\_C\_Q}$				mA
	VEEO Quiescent Current Setup C		$I_{EEO\_C\_Q}$				mA

Note 1: Exact power table conditions for pins may be found in XXX

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
POWER Setup D: HVDRIVE (High Voltage Driver with Deskew) Note 1							
	VCC Quiescent Current Setup D		$I_{CC\_D\_Q}$				mA
	VHH Quiescent Current Setup D		$I_{HH\_D\_Q}$				mA
	VCCO Quiescent Current Setup D		$I_{CCO\_D\_Q}$				mA
	VDD/A Quiescent Current Setup D		$I_{DD\_D\_Q}$				mA
	VEE Quiescent Current Setup D		$I_{EE\_D\_Q}$				mA
	VEEO Quiescent Current Setup D		$I_{EEO\_D\_Q}$				mA

DC Electrical Specifications – Calibration Buses

TABLE 5: DC ELECTRICAL SPECIFICATIONS - CALIBRATION BUSES

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
C12	EXT_FRC Voltage Range	Sweep to 1uA ?	V_{RNG_EXTFRC}	VEE + 1.0		VCC – 1.0	V
C13	EXT_SNS_HI, EXT_SNS_LO Voltage Range	Sweep to 1uA ?	$V_{RNG\_EXTSNS\_HI}$ $V_{RNG\_EXTSNS\_LO}$	VEE		VCC	V
C14	EXT_FRC Input Resistance		R_{IN_EXTFRC}	TBD		TBD	Ω
C15	EXT_SNS_HI/LO Output Resistance		R_{OUT_EXTSNS}	TBD		TBD	Ω
C16	EXT_FRC, EXT_SNS_HI, EXT_SNS_LO Leakage Current		$I_{LEAK\_EXTPINS}$	TBD		TBD	mA

DC Electrical Specifications – DUT Connection Pin

TABLE 6: DC ELECTRICAL SPECIFICATIONS - DUT CONNECTION PIN

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
C17	DOUT Hi-Z Leakage Current (–2V ≤ DOUT ≤ 6V)		I_{LEAK_DOUT}	TBD		TBD	nA
C18	DOUT Hi-Z Leakage Current (VEE ≤ DOUT ≤ VCC)		$I_{LEAK\_DOUT\_RAIL}$	TBD		TBD	nA
C19	DOUT Hi-Z Capacitance		C_{PIN_DOUT}		TBD		pF

DC Electrical Specifications – PPMU – Force Voltage

TABLE 7: DC ELECTRICAL SPECIFICATIONS PPMU - FORCE VOLTAGE

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
	Force Voltage Error	Measured after calibration. Valid for all min/max current in ranges.	FV_{ERROR}	–5		+5	mV
	Force Voltage Temperature Coefficient		FV_{TEMPCO}		200		µV/°C

DC Electrical Specifications – PPMU Force Current

TABLE 8: DC ELECTRICAL SPECIFICATIONS - PPMU FORCE CURRENT

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
	Force Current Error IR0 (±2µA Range) IR1 (±20µA Range) IR2 (±200µA Range) IR3 (±2mA Range) IR4 (±50mA Range)	Includes Common Mode Error. Measured after calibration.	FI_{ERROR}	 –10 –100 –1 –10 –250		 +10 +100 +1 +10 +250	 nA nA µA µA µA
	FI Temperature Coefficient		FI_{TEMPCO}		TBD		µA / °C

DC Electrical Specifications – PPMU Measure Voltage

TABLE 9: DC ELECTRICAL SPECIFICATIONS PPMU MEASURE VOLTAGE

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
	Measure Voltage Error	Measured after calibration.	MV_{ERROR}	–5		+5	mV
	Measure Voltage Temperature Coefficient		MV_{TEMPCO}		TBD		µV/ °C
	DGS, GND_REF Error		Ground Sense Error	–100		+100	µV

DC Electrical Specifications – PPMU Measure Current

TABLE 10: DC ELECTRICAL SPECIFICATIONS - PPMU MEASURE CURRENT

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
	Measure Current Error IR0 (±2µA Range) IR1 (±20µA Range) IR2 (±200µA Range) IR3 (±2mA Range) IR4 (±50mA Range)	Includes Common Mode Error. Measured after calibration	MI_{ERROR}	 –10 –100 –1 –10 –250		 +10 +100 +1 +10 +250	 nA nA µA µA µA
	MI Temperature Coefficient		MI_{TEMPCO}		TBD		µA/ °C

DC Electrical Specifications – PPMU Go-No-Go Comparator

TABLE 11: DC ELECTRICAL SPECIFICATIONS - PPMU GO-NO-GO COMPARATOR

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
	Threshold Error		CVA/B – $PPMU_{ERROR}$	–5		+5	mV
	Threshold Temperature Coefficient		CVA/B – $PPMU_{TEMPCO}$		20		µV/°C

DC Electrical Specifications – Voltage Clamp

TABLE 12: DC ELECTRICAL SPECIFICATIONS - VOLTAGE CLAMP

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
	Voltage Clamp Error, Calibrated	Measured through 50Ω	V_{ERR_VCLAMP}	–100		100	mV
	Voltage Clamp Temperature Coefficient		TC_{VCLAMP}		TBD		µV/°C
	Voltage Clamp Low Range		$V_{RNG\_VCLAMP\_LO}$	–2		3	V
	Voltage Clamp High Range		$V_{RNG\_VCLAMP\_HI}$	0		6	V
	Voltage Clamp DAC Resolution				100		mV

DC Electrical Specifications – Current Clamp

Current clamps are only for device gross protection, not precision control.

TABLE 13: DC ELECTRICAL SPECIFICATIONS - CURRENT CLAMP

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
	Current Clamp Error	Measured through 50Ω	I_{ERR_ICLAMP}	–5		5	mA
	Positive Current Clamp Threshold		I_{MAX_ICLAMP}	65	75	85	mA
	Negative Current Clamp Threshold		I_{MIN_ICLAMP}	–85	–75	–65	mA

DC Electrical Specifications – Resistor Values/Switch Impedances

TABLE 14: DC ELECTRICAL SPECIFICATIONS - RESISTOR VALUES/SWITCH IMPEDANCES

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
	EXT_FRC						
	EXT_SNS_HI, EXT_SNS_LO						

AC Characteristics

NOTE: For all of the following AC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Electrical Specifications – Differential Mode Comparator

All AC tests are performed after DC levels calibration; 1MHz, input transition time = 50ps, 20% to 80%; outputs terminated 50Ω to /VTTCx, comparator CLC set to 1/4 scale (010)

TABLE 15: AC ELECTRICAL SPECIFICATIONS - DIFFERENTIAL MODE COMPARATOR

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
	Propagation Delay	Note 1	T_{PD_DMC}		TBD		ps
	Propagation Delay TC	Note 1	TC_{PD_DMC}		TBD		ps/°C
	Propagation Delay Matching High Transition to Low Transition	Note 1	$T_{MATCHRF\_DMC}$		TBD		ps
	Propagation Delay Matching High to Low Comparator	Note 1			TBD		ps
	Minimum Detectable Pulse Width	V_{DUT0} = 0.0V, V_{DUT1} = –0.5V to +0.5V swing, drive termination mode, VIT = 0.0V, comparator threshold = 0.0V, greater than 50% output differential amp, repeat with VDUTx inputs reversed	T_{PWD_DMC}		TBD		ps
	Input Equivalent Rise/Fall Time VDUT0 = 0.0V, VDUT1 = –0.5V to +0.5V	V_{DUT0} = 0.0V, V_{DUT1} = –0.5V to +0.5V swing, drive termination mode, VIT = 0.0V, comparator threshold = 0.0V, comparator CLC set to max CLC setting repeat with VDUTx inputs reversed			TBD		ps
Propagation Delay Dispersion (VDUT0 = 0.0V, VIT = 0.0V, drive termination mode, repeat with VDUTx inputs reversed)							
	Slew Rate: 40ps vs. 1ns (20% to 80%)	V_{DUT1} = –0.5V to 0.5V swing, comparator threshold = 0.0V			TBD		ps
	Overdrive: 250mV vs. 750mV	Note 2			TBD		ps
	1.0V Pulse Width: 0.7ns, 1.0ns, 5.0ns, 10ns	V_{DUT1} = –0.5V to 0.5V swing, 32MHz, comparator threshold = 0.0V			TBD		ps
	0.5V Pulse Width: 0.6ns, 1.0ns, 5.0ns, 10ns	V_{DUT1} = –0.25V to 0.25V swing, 32MHz, comparator threshold = 0.0V			TBD		ps
	Duty Cycle 5% to 95%	V_{DUT1} = –0.5V to 0.5V swing, 32MHz, comparator threshold = 0.0V			TBD		ps

NOTES:

1. V_{DUT0} = 0.0V, V_{DUT1} = –0,5V to +0.5V swing, drive termination mode, VIT = 0.0V, comparator threshold = 0.0V, repeat with VDUXx inputs reversed,
2. For 250mV: V_{DUT1} = –0,0V to +0.5V swing; for 750mV V_{DUT1} = –0,0V to +1.0V swing, comparator threshold = –0.25V, repeat with VDUTx inputs reversed with comparator threshold = 0.25V

AC Electrical Specifications – PPMU Comparator

TABLE 16: AC ELECTRICAL SPECIFICATIONS - PPMU COMPARATOR

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
	Comparator Propagation Delay SENSE to CA/CB, Vsense = 0V to 1.0V Step, CVA = CVB = 0.5V Comparator A/Comparator B Delay Matching Delay Tempco		HS Comp TPLH, TPHL Δ(TPDLH/TPDHL) ΔTPD/°C		 TBD	TBD TBD TBD	ps ps ps/°C
	Comparator Minimum Pulse Width		CMPW	1			µs
	Comparator Output Rise/Fall Time (20% to 80% Amplitude		CA/CB Tr/Tf			TBD	ps
	Comparator Equivalent Bandwidth		Fmax	1			MHz
	Comparator Input Waveform Tracking (3V step, 100s Error, CVA/CVB = 0.6V to 2.6V)	See **Error! Reference source not found.**	Comp Wave Reconstruct	TBD			V/ns
Comparator Timing Dispersion							
	Common Mode Dispersion (DOUT_X Common Mode Voltage = –1V to 5V, DOUT_X Signal = 10MHz, 1Vpp square wave w/50% duty cycle, Tr/Tf = 1ns, CVA/CVB = 50% of square wave amplitude)	See **Error! Reference source not found.**	Δ(TPLH/TPHL)/V			TBD	ps

AC Electrical Specifications – Timing Deskew

TABLE 17: AC ELECTRICAL SPECIFICATIONS – TIMING DESKEW

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
	Coarse Element Delay	Room Temp			x		pS
	Medium Element Delay	Room Temp			x		pS
	Fine Element Delay	Room Temp			x		pS
	Rising edge adjustment unit delay	Room Temp			x		pS
	Falling edge adjustment unit delay	Room Temp			x		pS
	Maximum delay line achievable delay	Uncompensated, 50C		X			nS
	Minimum delay resolution	Uncompensated, 50C				X	pS
	Full Delay line drift, uncompensated	Char only, Tj 50 to 125	TC_{DLY_UNCMP}			X	pS / °C
	Full Delay line drift, compensated	Char only, Tj 50 to 125	TC_{DLY_COMP}			X	pS / °C

AC Electrical Specifications – Serial Interface

TABLE 18: AC ELECTRICAL SPECIFICATIONS - SERIAL INTERFACE

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
C11	SPI Clock Frequency		F_{MAX_SCLK}			50	MHz
C12	Chip Select Setup Time		T_{SU_CS}	5			ns
C13	Chip Select Hold Time		T_{HO_CS}	5			ns
C14	Serial Clock High Time		T_{PWH_SCLK}	6.7			ns
C15	Serial Clock Low Time		T_{PWL_SCLK}	6.7			ns
C16	Data In Setup Time		T_{SU_DIN}	2			ns
C17	Data In Hold Time		T_{HO_DIN}	4			ns
C18	Data Out Valid Time		T_{VAL_DOUT}	4			ns
C19	Data Out Hold Time		T_{HO_DOUT}	2			ns
C20	Data Out Tri-State		T_{TS_DOUT}	5			ns

AC Electrical Specifications – PPMU

TABLE 19: AC ELECTRICAL SPECIFICATIONS - PPMU

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
	PMU Settling Time, High Step (0 to +.5V, High Cload = 10nF, IR4)	PMU FV into pure Cload to ground. Last ring >5mV	$T_{STL\_HSTP/HC}$		100		µs
	PMU Settling Time, High Step (0 to 5V, Low Cload = 200pF, IR4)		$T_{STL\_HSTP/LC}$		70		µs
	PMU Settling Time, Low Step (100mV step, High Cload = 10nF, IR4)		$T_{STL\_LSTP/HC}$		60		µs
	PMU Settling Time, Low Step (100mV step, Low Cload = 200pF, IR4)		$T_{STL\_LSTP/LC}$		50		µs

Chip Overview

The Hood is a highly integrated System-on-a-Chip (SoC) pin electronics solution that incorporates every analog function, along with digital support circuitry required to create 8 independent pin channels for Automated Test Equipment. Each channel is configured via a 100MHz SPI interface, and all real time data is programmed and read back through high speed FLEX I/O pins that can be configured to interface directly to other devices using multiple single-ended and differential logic families.

The Hood has extremely low power dissipation, small footprint, combined with flexibility to enable low power testers with high pin counts.

SPI (Serial Programmable Interface)

All chip setup, configuration control, and writing to and reading back of the internal registers is controlled through the 4-bit serial SPI port. The SPI port is typically used to setup the operating mode of the chip prior to executing a test, or to change modes during a test.

An internal register chart in this datasheet documents all programmable control signals and their addresses and shows how to program each interal signal.

Analog Reference

All on-chip analog functions are related to one of several off-chip precision reference inputs:

- VREF
- RREF

These external references are used to provide accurate and stable analog circuit performance that does not vary over time, temperature, supply voltage, or process changes.

External Signal Nomenclature

All input and output pins, when referred to in the datasheet or in any circuit diagram, use the following conventions:

- All capital letters (i.e., EXT_SNS)
- Underscores for clarity (i.e., EXT_FRC)
- Shown next to an I/O circle in any schematic
- Pound sign used to signify that the signal name applies to all channels (i.e., DATA_P_#)

SPI Programmed Control Line Nomenclature

Any internal signal, DAC level, or control signal that is programmed via the SPI port uses a different nomenclature:

- All letters in the word are capitalized.
- Underscores are used for clarity.
- Not shown with an I/O Pin in any schematic.

Control lines, internal registers, and other inputs are defined in the Host Serial Bus Data section and listed in Register Map section of this datasheet.

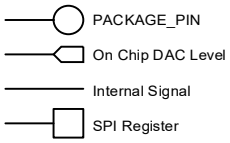

FIGURE 3: DATASHEET NOMENCLATURE

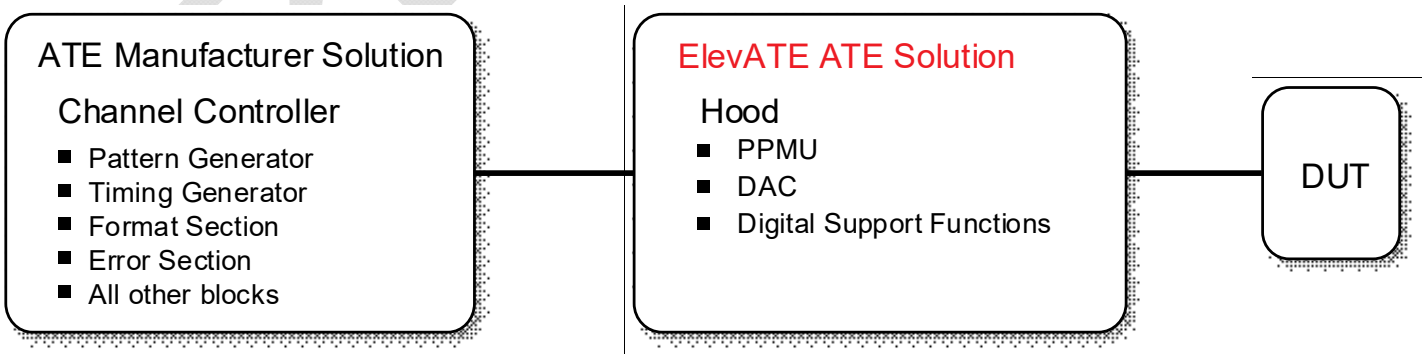

FIGURE 4: ELEVATE ATE SOLUTION

PMU Block Diagram

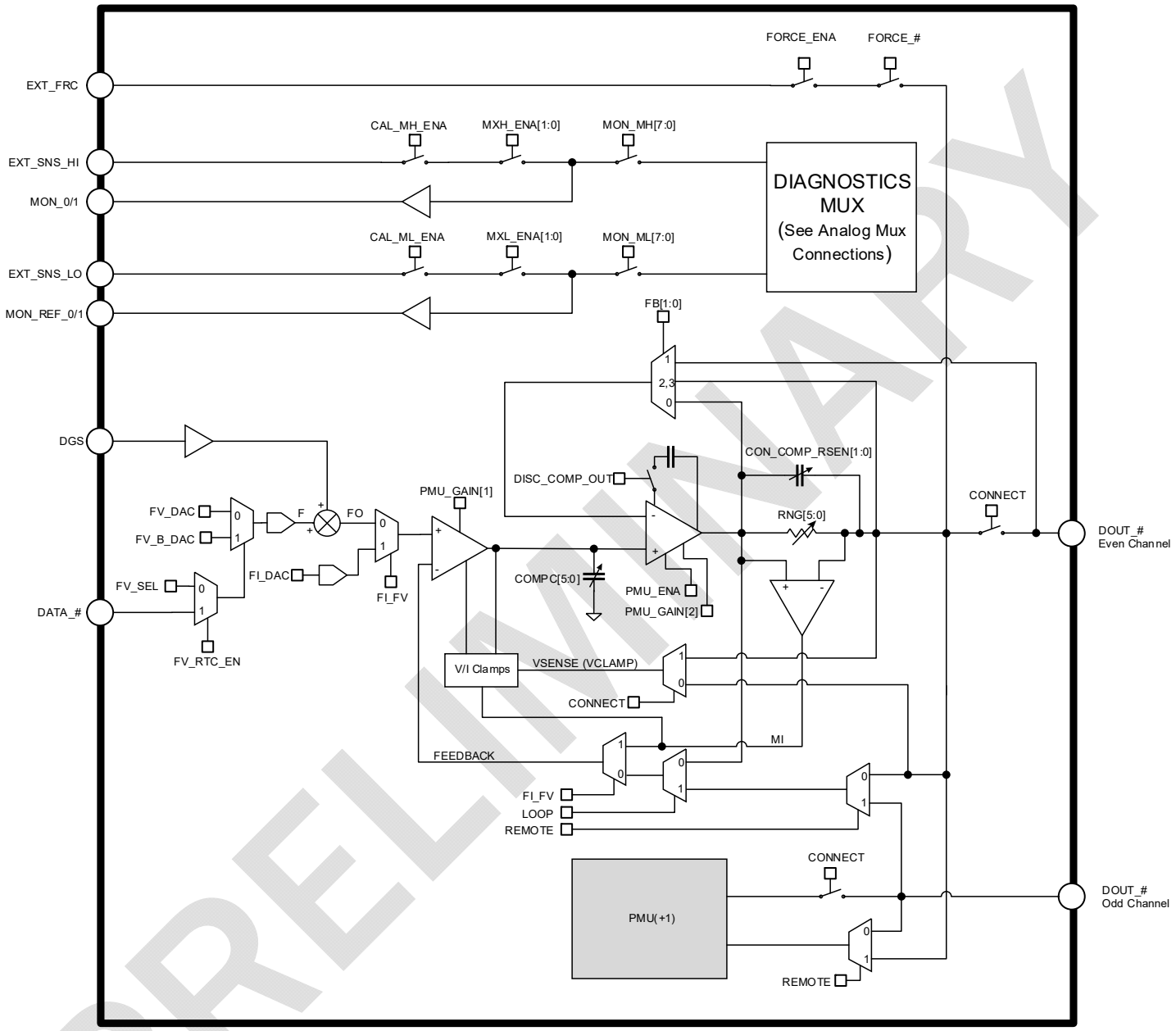

FIGURE 5: PPMU BLOCK DIAGRAM

Measure and Diagnostic Block Diagram

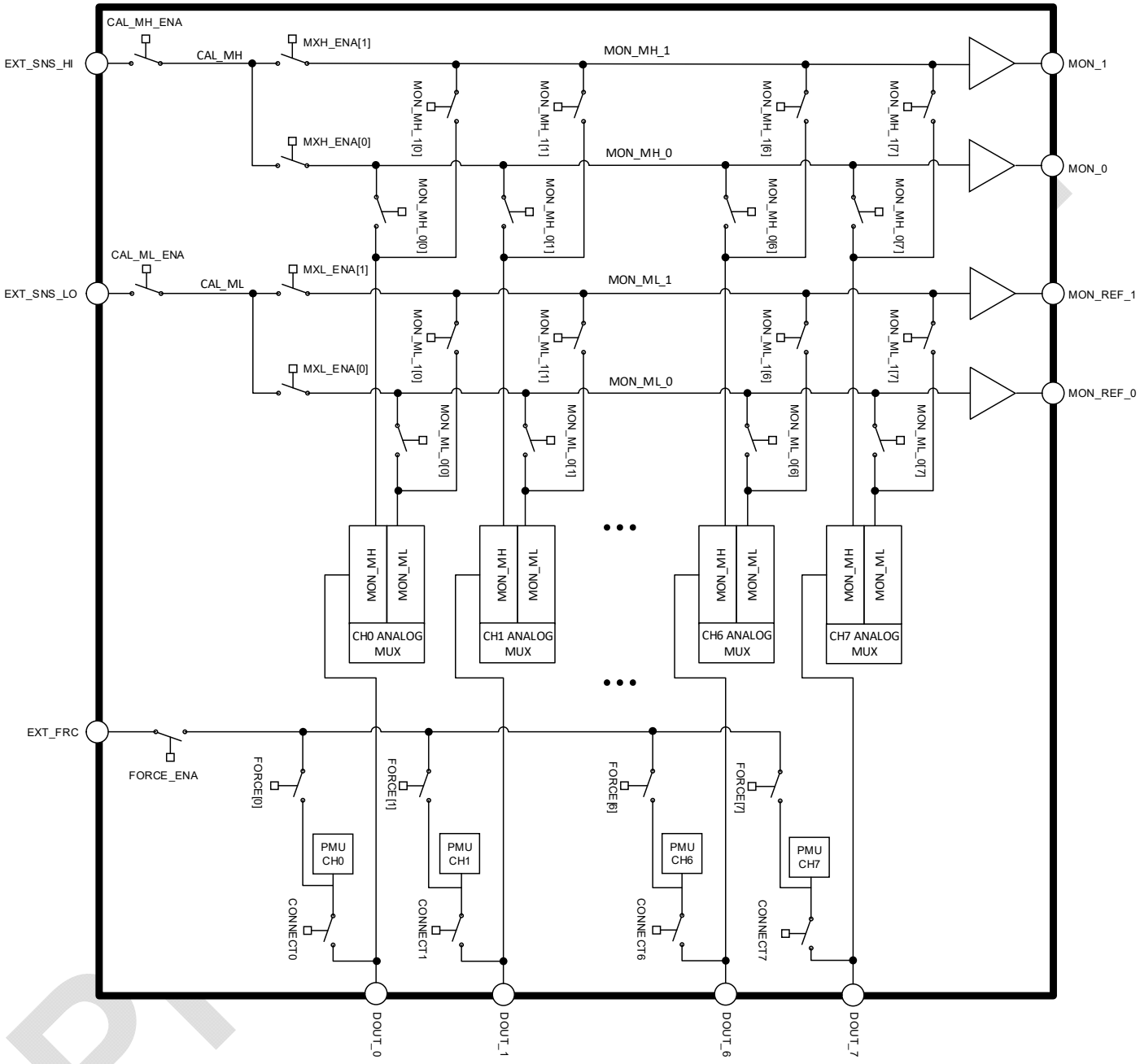

FIGURE 6: MEASURE AND DIAGNOSTIC MUX DIAGRAM

PPMU Overview

Each channel has a per-pin parametric measurement unit with the ability to:

- Force Current (FI)
- Force Voltage (FV)
- Measure Current (MI)
- Measure Voltage (MV)

The current or voltage measured by the PPMU may be tested via two different mechanisms:

- On-board PMU window comparator
- An analog output voltage available on the analog test and calibration buses.

High Impedance

The forcing op amp may be placed into a HiZ state, although care should be exercised when doing this due to the large transient response possible when turning the op amp back on.

TABLE 20: PMU_ENA

PMU_ENA	CH # FORCING OP AMP STATUS
0	HiZ
1	Active

Setting PMU_ENA to 0 powers off the forcing op amp and reduces quiescent power consumption. However, the recommended PMU HiZ function is through the CONNECT switch.

TABLE 21: CONNECT

CONNECT	SWITCH
0	Open
1	Closed

A 200K Ω resistor can be connected from FORCE to GND. This resistor can be connected or disconnected using the DUTSAFE register. This resistor is used to bleed off any small currents on the force line when in the High Impedance state.

TABLE 22: DUTSAFE

DUTSAFE	200K Ω Resistor
0	Disconnected
1	Connected

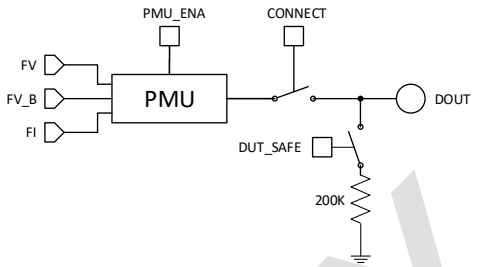

FIGURE 7: PMU ENABLE, CONNECT, AND DUTSAFE

When disabled through the CONNECT switch, the PMU maintains an extremely low leakage current when DOUT remains between the two analog supply levels, VCC and VEE.

FIGURE 8: HIGH IMPEDANCE

PPMU Operating Mode

The decision whether to force current or voltage, or to measure current or voltage, is controlled by the SPI port. There are no restrictions between Force Voltage and Force Current and Measure Voltage and Measure Current in that all combinations are legal modes.

TABLE 23: PPMU OPERATING MODE

FI_FV	PPMU FORCE FUNCTION
0	FV
1	FI

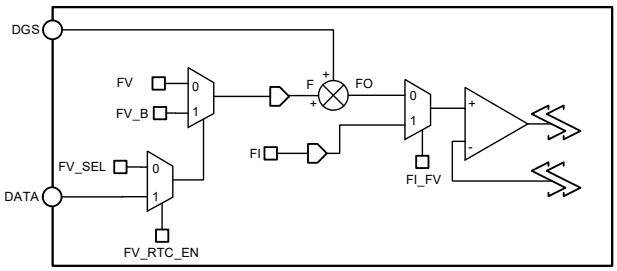

FIGURE 9: PPMU FV/FI

Force Voltage

In FV mode, the voltage at DOUT is offset and will track any voltage changes on the DGS pin. The DGS pin should be connected to the gound of the device under test.

The resulting forcing voltage is FO = F + DGS. This is shown above in **Error! Reference source not found.**.

Force Voltage Input Source

The Force Voltage input to the main forcing op amp can be sourced from either the FV or FV_B register level inputs. This selection can be made by the SPI port or by use of the external DATA pins. By using the DATA pins, the Force Voltage op amp can be switched between the FV and FV_B levels without writing any registers.

TABLE 24: FV_RTC_EN

FV_RTC_EN	FV_SEL	DATA	F
0	0	X	FV
0	1	X	FV_B
1	X	0	FV
1	X	1	FV_B

Current Ranges

The PMU can force current over 50mA. In order to achieve the maximum accuracy while still being able to measure small currents, five current ranges are supported.

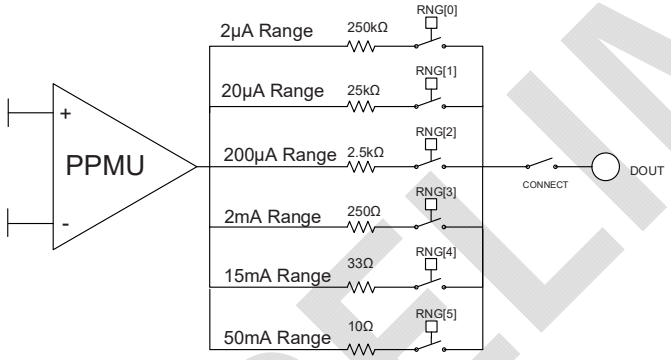

FIGURE 10: CURRENT RANGES

TABLE 25: PMU RNG

PMU_TERM_ENA	RNG[5:0]	CURRENT RANGE	IMAX*	RSENSE
0	000001	IR0	±2µA	250kΩ
0	000010	IR1	±20µA	25kΩ
0	000100	IR2	±200µA	2.5kΩ
0	001000	IR3	±2mA	250Ω
0	010000	IR4	±15mA	33Ω
0	100000	IR5	±50mA	10Ω

*Imax of a current range is defined as the current that creates a 500mV drop across the sense resistors. There is no hard limit within the part in that currents that exceed Imax will simply continue to create a large sense voltage.

The PMU_TERM_ENA bit must be set to '0' for the RNG bits to have any effect on the range switches. This bit, when set to '1', puts the PPMU into termination mode and is discussed later in this datasheet.

The SPI selects the current range by setting the range select bit high. Each range select bit has independent control, allowing a wide variety of "make before break" options when changing current ranges.

It is possible to select more than one range simultaneously. However, this option should be used only when changing ranges as a means of controlling the transient response associated with changing ranges or changing modes.

Activating more than one range simultaneously will have the effect of placing the sense resistors in parallel thus altering the transfer function. Activating more than one range at the time is not recommended for taking measurements.

Measure Current

The current across the sense resistor will create an analog voltage that is proportional to the current flowing through DOUT. Imax is determined by the current range selection. There is a transfer function between the current at the DOUT pin and the voltage measuring the current at the MON pins.

TABLE 26. MEASURE CURRENT TRANSFER FUNCTION

Voltage across Sense Resistor	I_{OUT}
Reference Voltage – 500mV	–Imax (Sinking current)
Reference Voltage V	0
Reference Voltage + 500mV	+Imax (Sourcing current)

*The reference voltage for the measure current transfer function is dependent on how current is measured. The reference voltage can either be 2.25V or GND_REF.

There are three options for measuring current in the Hood chip. Each of these options use the Monitor and Diagnostics

buses discussed later in this datasheet.

- MI Output – The MI Output has a voltage reference of 2.25V. When no current is measured, the output voltage is 2.25V. For each selected current range, the voltage can vary +/-500mV depending on whether the PMU is sourcing current or sinking current.
- MI Output 2X – This option is the same as MI Output except the voltage swing is double to +/-1V.
- MI Input+/MI Input – Voltage reference for this option is GND. A differential measurent between MI Input+ and MI Input- will vary from +500mV to -500mV.

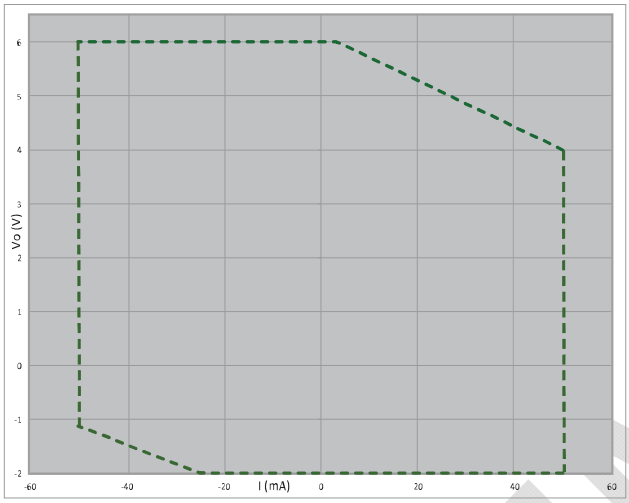

FIGURE 11: PPMU COMPLIANCE CURRENT

PPMU Architecture

The PPMU is made up of a two op-amp output stage architecture. The two stages are: Input op-amp and the output op-amp:

- The output op-amp is low gain so it can respond quickly to changes in the ouput.
- The input op-amp is high gain to provide a more accurate voltage.

With this architecture, there are feedback options for:

- Total PPMU including both output stages.
- Output op-amp stage.

Total PPMU Voltage Feedback

There are multiple voltage feedback nodes to the inverting input of the forcing op amp. The forcing op amp is automatically protected against going open loop when the DPS goes into HiZ.

TABLE 27: VOLTAGE FEEDBACK OPTIONS

LOOP	PMU_ENA	FI_FV	CONNECT	REMOTE	MODE
0	X	X	X	X	Tight Loop
X	0	X	X	X	HiZ
X	1	1	X	X	FI
1	1	0	1	0	Local Sense
1	1	0	1	1	Remote Sense
1	1	0	0	X	Open Loop Not Suggested

Tight Loop Feedback

With Loop = 0, the forcing op amp will be configured as a unity gain amplifier tracking FV. This tight loop is the default condition upon reset or power-up.

The tight loop configuration is NOT used for any traditional PMU FI or FV function. It is used mainly for:

- A stable default condition
- Resistive load applications

Local Sense Feedback

The inverting feedback to the main forcing op-amp is at the DOUT pin. This will normally be the Feedback option used.

Remote Sense Feedback

Adjacent channels can be arranged in pairs to support a PMU remote sense mode. In remote sense mode the output of one channel is used to force voltage while the DOUT pin of the other adjacent channel is used as a remote voltage sense input. Either channel in the adjacent pair can be used to as the forcing pin while the other channel's pin is used for remote sense. This option ensures the most accurate voltage at the load by eliminating IR drops caused by trace resistance but uses two output pins to accomplish.

TABLE 28: REMOTE FEEDBACK

REMOTE	Feedback
0	Local sense will be selected at DOUT pin.
1	Sense is connected to the adjacent channel DUT pin. Adjacent odd/even channels can be used to for and sense voltage at the DUT.

Output Op-Amp Voltage Feedback

There are three voltage feedback nodes to the inverting input of the output op-amp. The output op-amp is located just after the internal PPMU compensation caps.

TABLE 29: FB OPTIONS

FB[1:0]	Feedback
00	Feedback from the amplifier output. This is the internal side of the sense resistor.
01	Feedback is from DOUT pin. If this option is used, the CONNECT switch is in the feedback path and should always be closed.
1X	Feedback is from just inside the CONNECT switch. This is the recommened FB for all PPMU use and is the default connection.

FB[1:0] = 1X is the default setting for the FB register and is recommended for all use. It has been seen when changing this option during use, a glitch can been seen on the output.

Force Current

FI Voltage Clamps

Each PMU has a set of programmable voltage clamps that limit the swing of the forcing op amp feedback voltage (Vsense) when the PMU is forcing current. These clamps protect the DUT when current is being forced into a high impedance node at the DUT. There are independent clamps for both High Voltage and Low Voltage. The voltage clamps are only available in Force Current mode.

The internal current clamps override the the PMU voltage only and do not limit external sources.

The clamps may be turned off by setting CLL_DIS = 1 and CLH_DIS = 1, in which case the clamps have no effect while DOUT varies between the supply voltages, VCC and VEE. CLL_DIS disables the low voltage clamp, CLH_DIS disables the high voltage clamp. The CLH_DIS/CLL-DIS register bits are shared with both the voltage clamps and current clamps.

TABLE 31: CLL/CLH_DIS

CLL/CLH_DIS	Vsense	VOLTAGE CLAMPS
1	X	Not Active
0	Vsense > CLH	DOUT = CLH
0	Vsense < CLL	DOUT = CLL
0	CLL < Vsense < CLH	Not Active

When active, if the sensed voltage exceeds the high or low voltage clamp, the PMU reduces the output current in order for the output voltage to not exceed the clamp. If the voltage subsequently returns back to within the clamp thresholds, the PMU resumes forcing the programmed current.

The PMU voltage clamps are programmable with an 8-bit DAC. These can be set anywhere within the operable range of the Pin Electronics.

In FI Mode, the following transfer function translates the current measured across a chosen RNG resistor into an output current. The output of the MI instrumentation amplifier is used as the feedback to the forcing output amplifier. The DAC level voltages in FI mode match the voltages across the RNG resistors. Programmable current is mapped as shown below. The FI_FV bit must be set to '1' for Force Current Mode.

TABLE 30: FORCE CURRENT DAC CODES

DAC Code	IOUT
FFFF	+Imax (Sourcing)
7FFF	0
FFFF	-Imax (Sinking)

TABLE 32: PMU VOLTAGE CLAMP LOW

CLL[7:0] Bit[7] Unused	PMU VOLTAGE CLAMP LOW
00000000	-2.2V
•	•
•	•
01111111	4.0V

TABLE 33: PMU VOLTAGE CLAMP HIGH

CLH[7:0] Bit[7] Unused	PMU VOLTAGE CLAMP HIGH
00000000	0.0V
•	•
•	•
01111111	6.2V

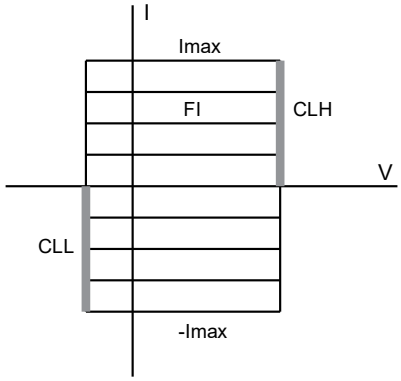

FIGURE 12: VOLTAGE CLAMP

FV Current Clamps

Each PMU had 2 ranges of programmable current clamps that limit the amount of current flow when the PMU is forcing voltage. These clamps are useful in protecting the DUT from an over current situation. There are independent

clamps for both sourcing and sinking. The Current Clamps are only available when the PMU is in Force Voltage mode.

The 2 current clamp ranges correspond to the 2 upper PMU current ranges:

- 50mA range (8-bit setting)
- 2mA range (3-bit setting)

In the current ranges less than 2mA, the current is self-limited to the voltage drop caused by the output current and sense resistor (RSENSE).

The clamps may be turned off by setting CLL_DIS = 1 and CLH_DIS = 1, in which case the clamps have no effect while DOUT varies between the supply voltages VCC and VEE. CLL_DIS disables the sinking clamp, CLH_DIS disables the sourcing clamp. The CLH_DIS/CLL-DIS register bits are shared with both the voltage clamps and current clamps.

TABLE 34: CURRENT CLAMPS

CLL_DIS CLH_DIS	Current	CURRENT CLAMPS
1	X	Not Active
0	Current > ICH	DOUT = ICH
0	Current < ICL	DOUT = ICL
0	CLL < Current < CLH	Not Active

When active, the Current Clamps sense the current supplied by the PMU. If the current is within the boundaries set by the clamps, not action is taken. If the measured current exceeds the upper or lower current clamp, the PMU reduces the output voltage in order for the outuput current to not exceed the clamp. If the current subsequently drops back to within the clamp levels, the PMU resumes forcing its programmed voltage.

The internal current clamps override the the PMU current only and do not limit external sources.

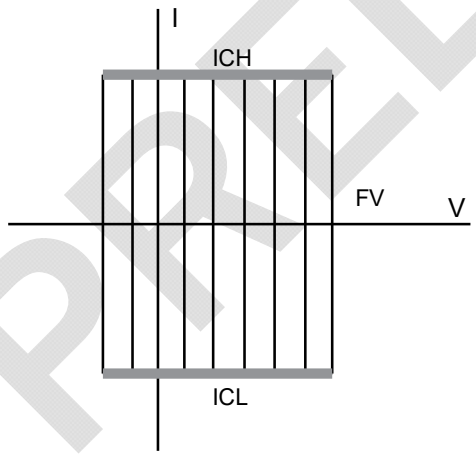

FIGURE 13: CURRENT CLAMPS

The 2 current clamp ranges are separated into sourcing and sinking registers.

TABLE 35: CURRENT CLAMP REGISTER SETTING

REGISTER	CURRENT	CURRENT CLAMP RANGE
ICH_IR50m[7:0]	50mA Sourcing	~2mA to 70mA
ICL_IR50m[7:0]	50mA Sinking	~-2mA to -70mA
ICH_IR2m[2:0]	2mA Sourcing	~ 3mA
ICL_IR2m[2:0]	2mA Sinking	~ -3mA

The 50mA clamp allows the user to set the clamp levels greater than the max current range and get down to about +/- 2mA.

The 2mA clamp is a coarse clamp that is intended to be calibrated to 3mA and left there just for gross DUT protection.

PPMU Termination Mode/Resistive Load

The PMU may be connected and disconnected through the SPI port in order to provide a resistive load. This gives the user an option for a termination resistance with different values than the 50Ω termination available from the PE driver. The PPMU terminations are not intendeded to be provide good RF termination. Connections available for termination mode only are not allowed when when measuring current.

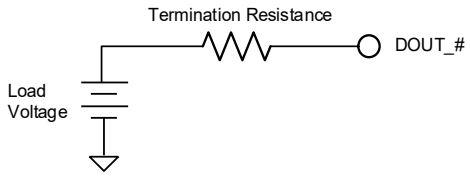

FIGURE 14: PPMU TERMINATION

LOAD VOLTAGE

To establish the load voltage source, the following is recommended.

- FI_FV = 0 (FV mode)
- FV/FV_B = Desired Termination Voltage
- Loop = 0 (Tight Loop)

The forcing op amp will now be a low impedance voltage source.

PPMU Termination Mode

The resistance between the load voltage and DOUT will be the series combination of the resistors, switch resistances, and termination mode resistors. The combination of resistances depends on the which termination mode is used and how much resistance is needed.

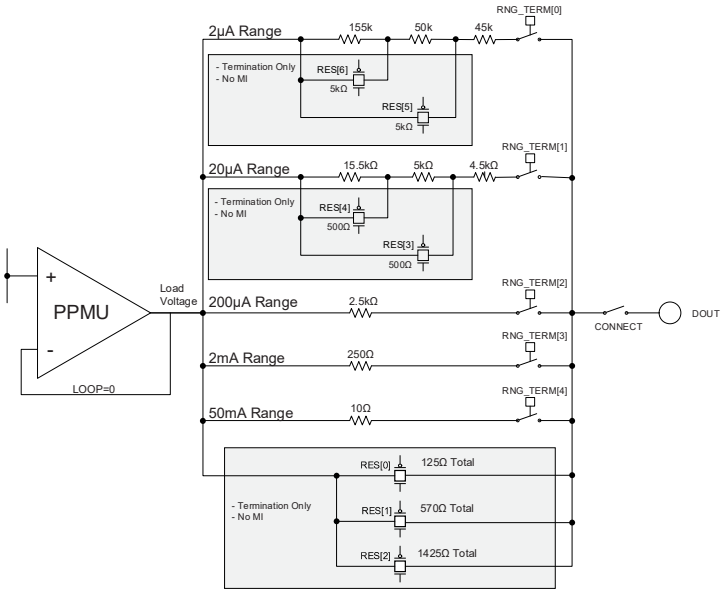

FIGURE 15: PPMU TERMINATION MODE

To enable Termination Mode, PMU_TERM_ENA must be set to '1'.

TABLE 36: PMU_TERM_ENA

PMU_TERM_ENA	PMU# TO DOUT_#
0	Normal PMU operation. PPMU resistors set by RNG[5:0] bits.
1	PPMU Termination Mode enabled. Termination resistors set by RES[5:0] bits.

When PPMU Termination Mode is enabled (PMU_TERM_ENA = 1), range control for the PMU resistors switches over to the RNG_TRM[5:0] register bits. When PMU_TERM_ENA is disabeled (PMU_TERM_ENA = 0), all the RNG_TERM bits are forced to '0' and control of the PPMU resistors is set by the RNG[5:0] bits.

TABLE 37: RNG_TRM

PMU_TERM_ENA	RNG_TRM [5:0]	CURRENT RANGE	IMAX*	RSENSE
1	000001	IR0	±2µA	250kΩ
1	000010	IR1	±20µA	25kΩ
1	000100	IR2	±200µA	2.5kΩ
1	001000	IR3	±2mA	250Ω
1	010000	IR4	±50mA	10Ω

Additional termination resistances can be added using the RES[5:0] bits. These bits can only be used in PPMU Termination Mode (PMU_TERM_EN = '1'). When PMU_TERM_ENA is disabeled (PMU_TERM_ENA = 0), the RES[5:0] bits are ignored.

TABLE 38: RES[6:0] BITS

PMU_TERM_ENA	RES[6:0]	RESISTANCE	TERMINATION RESISTANCE
1	RES[0]	125Ω	125Ω
1	RES[1]	570Ω	570Ω
1	RES[2]	1425Ω	1425Ω
1	RES[3]	500Ω	5KΩ When used in Conjunction with RNG_TRM[1]
1	RES[4]	500Ω	10KΩ Used in Conjunction with RNG_TRM[1]
1	RES[5]	5KΩ	50KΩ Used in Conjunction with RNG_TRM[0]
1	RES[6]	5KΩ	100KΩ Used in Conjunction with RNG_TRM[0]

PMU Compensation

The PMU has variable compensation capacitor settings which can be changed to:

1. Be more stable under large capacitive loads.
2. Have a faster settling transient response when the DUT undergoes a change in load currents.

These settings will allow the adjustment of the internal dominant pole for optimal stablitity. This must be lower than the pole created by the sense resistor and load capacitor. Switching in the compensation can cause glitches, therefore it is best to do this when the PMU is disconnected (CONNECT = 0). There is a trade-off between stability and transient response performance. The larger the compensation capacitor, the more stable the PMU will be. However, the response settling times will be slower.

TABLE 39: COMPC

COMPC[4:0]	VALUE
00001	10pF
00010	20pF
00100	40pF
01000	70pF
10000	150pF

The compensation capacitors are in parallel and can be used in any combination. When 2 or more are selected, the compensation capacitance is additive.

Recommended settings:

For Cload ≤ 150pF use 0b11000

For Cload ≤ 0.1uF use 0b11111

Output Op-Amp Compensation

The PMU has internal compensation capactitors for local feedback loop stability. These caps can be disconnected to trade response time for stability. The internal compensation can be enabled or disabled as follows:

TABLE 40: DISCONNECT OUPUT COMPENSATION

DISC_COMP_OUT	COMPENSATION
0	Connected
1	Disconnected

Rsense Compensation

Compensation capacitors can be connected across the Rsense range resistors to further fine tune settling response. It is recommended that both bits be set to "1".

TABLE 41: RSENSE COMPENSATION

CON_COMP_RSEN[1:0]	OUTPUT COMPENSATION
11	Recommended Setting

PMU GM

The PMU GM bit increases the ouput stage bias current by ~10X. This is relatively small for the 2uA to 15mA ranges, but is substantial for the 50mA range (~17mA). The

Current clamps are used to identify an overcurrent situation and raise a flag.

improvement in stability and settling times is substantial with this setting and is necessary to get stable operation at the 2uA range and 20uA range, but is not needed for 50mA. This bit should be set to "1" for the 2uA to 15mA ranges and set to "0" for the 50mA range.

TABLE 42: PMU_GAIN

PMU_GM	RECOMMENDED SETTINGS
0	50mA Range
1	2uA to 15mA Ranges

PMU Gain Control

Gain control within the PMU can be fined tuned to aid in stability and settling times. The PMU_GAIN[1:0] register bits can change the gm (open loop gain) of several operational amplifiers within the PMU.

TABLE 43: PMU GAIN CONTROL

PMU_GAIN[3:0]	GM SETTINGS
Bit 0	Decreases the gm of the clamp
Bit 1	Decreases the gm of the PMU input stage

TABLE 44: RECOMMENDED PMU GAIN CONTROL SETTINGS

PMU_GAIN1:0]	GM SETTINGS
00	All current ranges

Monitor and Diagnostics

A group of five analog test and calibration buses are implemented for various use measurements. These buses are used to route several internal diagnostic nodes and measure voltages to external pins that can be measured for test, calibration, and diagnostic analysis. The pins that can be connected to these buses are: MON_1, MON_0, MON_REF_0, MON_REF_1, EXT_SNS_HI, EXT_SNS_LO, EXT_FRC. There are internal switches controlled through the SPI port that make each one of these connections possible. The buses and usage are listed below.

TABLE 45: MEASUREMENT AND CALIBRATION BUS

Measurement and Calibration Bus	Usage
FORCE	Connects the DOUT_# output to the EXT_FRC pin.
CAL_MH	Connects the MON_MH_ bus to the EXT_SNS_HI pin
CAL_ML	Connects the MON_ML[X] bus to the EXT_SNS_LO pin.
MON_MH_#	Connects to the positive ouput of the selected channel diagnostic mux. Can be connected to the MON_# pins or to the CAL_MH bus.
MON_ML_#	Connects to the negative ouput of the selected channel diagnostic mux. Can be connected to the MON_REF_# pins or to the CAL_ML bus.

MON_MH and MON_ML Buses

- There are two MON_MH and two MON_ML buses. The MON_MH_0 and MON_ML_0 buses connect to the ouput pins MON_0 and MON_REF_0. The MON_MH_1 and MON_ML_1 buses connect to the ouput pins MON_1 and MON_REF_1.
- The MON_MH_0 and MON_MH_1 buses can be connected to the CAL_MH bus using the MXH_ENA[X] register bits.
- The MON_ML_0 and MON_ML_1 buses can be connected to the CAL_ML bus using the MXL_ENA[X] register bits.
- The MON_MH_0, MON_MH_1, MON_ML_0, and the MON_ML_1 buses are connected to output pins as listed in Table 46 below. These buses are connected to the external pins using unity gain buffers. These buffers are added to be able to drive an external load and prevent IR drops across external switches which induce measurement error.

TABLE 46: MON_MH/MON_ML PIN CONNECTIONS

BUS	PIN CONNECTION
MON_MH_0	MON_0
MON_MH_1	MON_1
MON_ML_0	MON_REF_1
MON_ML_1	MON_REF_1

MON_MH and MON_ML Transfer Function

When measuring voltage, the MON_MH/MON_ML buses have a 1:1 transfer function with the voltages they are measuring. When measuring current, MON_MH/MON_ML varies ±500mV from a reference voltage depending on whether it is measuring -Imax or +Imax.

TABLE 47: MON_MH/MON_ML TRANSFER FUNCTION

MODE	MON_MH/MON_ML	DOUT
MV	Voltage at DOUT.	DOUT
MI	Reference Voltage - 1V	-Imax
MI	Reference Voltage	0
MI	Reference Voltage + 1V	+Imax

*The reference voltage can be selected as either GND_REF or 2.25V.

FORCE Bus

The FORCE bus is used to connect the DOUT_X pin to the EXT_FRC pin. This is a low impedance path which can be used for voltage or current calibration. To connect the DOUT_X pin to the EXT_FRC pin, both the FORCE[X] and the FORCE_ENA switches must be closed using the SPI port.

TABLE 48: FORCE_ENA

FORCE_ENA	FORCE Bus
0	FORCE bus disconnected from EXT_FRC pin
1	FORCE bus connected to EXT_FRC pin

CAL_MH and CAL_ML Buses

The CAL_MH bus is used as an interconnect between the MON_MH buses and the EXT_SNS_HI pin. EXT_SNS_HI is connected/disconnected using the CAL_MH_ENA bit. The CAL_ML bus is used as an interconnect between the MON_ML buses and the EXT_SNS_LO pin. EXT_SNS_LO is connected/disconnected using the CAL_ML_ENA bit. These connections are used during calibration and other voltage measurements.

TABLE 49: CALMH_ENA

CAL_MH_ENA	CAL_MH Bus
0	CAL_MH bus disconnected from EXT_SNS_HI pin
1	CAL_MH bus connected to EXT_SNS_HI pin

TABLE 50: CALML_ENA

CAL_ML_ENA	CAL_ML Bus
0	CAL_ML bus disconnected from EXT_SNS_LO pin
1	CAL_ML bus connected to EXT_SNS_LO pin

Analog Mux Connections

TABLE 51 AND

TABLE 51: ANALOG MUX CONNECTIONS - MON__SEL

MON_SEL[4:0]	Signal
0	No Connect
1	DUT outputfoot
2	FV Mux Output
3	MI Output
4	MI Input +
5	OTA-INN
6	Main Loop Fdbk
7	OTA Output
8	Vclamp ref low
9	Vclamp ref high
10	Vsense clamp
11	Inn
12	GND_REF
13	MI Output 2X
14	Sense Pad Voltage
15	DUT Remote Sense Voltage
31	Temperature VB

Table 52 below list analog nodes accessible through the MON_MH and MON_ML calibration busses.

- Use the MH_SELGP[1:0] and MH_SEL bits[4:0] to connect to the MON_MH busex.
- Use the ML_SELGP[1:0] and ML_SEL bits[4:0] to connect to the MON_ML buses.

MH_SEL[1:0] and ML_SEL[1:0] bits select which subgroup (column) of the analog nodes will be selected.

MH_SEL[4:0] and ML_SEL[4:0] select which node within each subgroup will be selected.

Pins

MON_REF is a reference signal used as the inverting input to a differential off-chip ADC. The SPI port selects the reference signal as well as controls the high impedance function.

Analog Mux Connections

TABLE 51: ANALOG MUX CONNECTIONS - MON__SEL

MON_SEL[4:0]	Signal
0	No Connect
1	DUT outputfoot
2	FV Mux Output[1]
3	MI Output[2]
4	MI Input +[3]
5	OTA-INN
6	Main Loop Fdbk
7	OTA Output
8	Vclamp ref low
9	Vclamp ref high
10	Vsense clamp
11	Inn
12	GND_REF
13	MI Output 2X[4]
14	Sense Pad Voltage
15	DUT Remote Sense Voltage
31	Temperature VB

TABLE 52. ANALOG MUX CONNECTIONS – MON_REF_SEL

MON_REF_SEL[4:0]	Signal
0	No Connection
1	DUT_GND
2	GND_REF
3	2.25V Instrumentation Amplifier Reference[5]
4	MI Input-
5	VDD[6]
6	GND
7	VCC/2
8	VEE
9	VHH/4
10	Clamp Hi Flag
11	Clamp Lo Flag
12	I shutoff
13	ML_fb_input
14	pmu_input_inverted
15	pmu_input_buf
31	Temperature VA

[1] FV Mux Output. Mux is used to access internal DAC voltages and force them at the PMU output. Source is selected with register PMU_TESTMODE.

[2] Reference for MI Output is 2.25V.

[3] Reference for MI Input+ is MI Input -. The ADC is doing the difference measurement. Common Mode range for MI Inp and MI Inn is approx. -1.5 to 5.5 V.

[4] Reference for MI Output is 2.25V. This MI measurement has a gain of 2.

[5] 2.25V Reference on ADC_ML can be measured relative to GND_REF on ADC_MH.

[6] ML_Sel choices 5-12 on the PMU are all internal diagnostic test points for the PMU. The reference is GND_REF on ADC_MH. Voltages measured will be opposite signed but the ATE is able to deal with that.

External Components and Temp

Temperature Sensing

There are four sets of temperature diodes on chip that can be muxed to the MON_MH and MON_ML buses using the SPI port. These buses are discussed in the Monitor and Diagnostics section above. The temperature measurement is a differential voltage with two voltages being generated with matched diodes. Each of these matched diodes is driven with a different current. The two voltages generated create a transfer function that track the internal junction temperature of the Hood device. All circuitry and currents for temperature measurements are generated on chip.

As mentioned above, there are four sets of temperature diodes. Each set is shared between 2 adjacent channels (Channels 0/1, 2/3, 4/5, 6/7). Therefore, if measuring the temperature on 2 adjacent channels, the user would read the same temperature.

The two internally generated voltages are:

- Temp Va
- Temp Vb

When measured, these may be used to calculate the junction temperature associated with the set of diodes as shown in the following equation.

$$TJ[^{\circ}C] = 1987 \cdot (Va - Vb) - 273$$

The on-chip temperature sensor provides a means for monitoring the relative temperature change of the IC. It is not intended for absolute temperatue measurements.

Dut Ground Sense (DGS)

The actual ground reference level at the DUT may be different than that used by the DAC reference. DGS is a high impedance analog voltage that provides a means of tracking the destination ground and making an additional offset to the programmed level so the programmed level is correct with respect to the DUT. There is only one DGS input pin per chip.

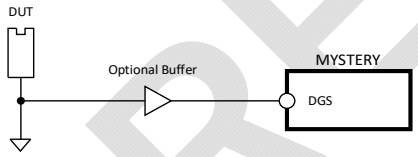

FIGURE 16: DUT GROUND SENSE

The input at DGS should be:

- Filtered for noise
- Stable
- Reflect the actual ground at the DUT

DGS is not added into the DC level when measuring a current by the PMU or forcing a current.

Required Off Chip Components

A precision voltage reference level and external resistor is required per chip. However, there may be a need for decoupling capacitors on the power supply pins. The need for decoupling capacitors is dependent upon the particular application and is therefore system dependent.

VREF

VREF is an analog input voltage this is used to program the on-chip DC levels. VREF should be held at +1.25V with respect to GND. There is one VREF pin shared by all channels on the same chip. This pin is a high impedance CMOS gate input.

RREF

RREF is a 12.4KΩ precision external resistor used to control various internal bias current.

VCCO and VEEO

VCCO and VEEO are the positive and negative power supplies for the output stage during high current operation. In order to minimize power consumption in high current, low voltage applications, VCCO and VEEO should be as low as possible while still maintain adequate headroom.

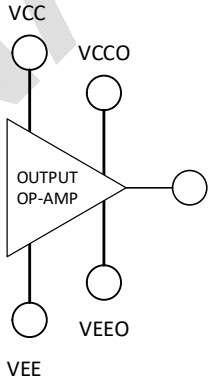

FIGURE 17: VCCO AND VEEO SUPPLIES

Power Supply Restrictions

The following guidelines must be met to support proper option:

1. VEEO, VEE <= GND
2. VCC <= VHH
3. VCCO <= VCC
4. VDD, VDDA <= VCCO
5. VEE <= VEEO

Schottky diodes are recommended on a once per board basis to protect against a power supply restriction violation. The diodes will protect against power supply failure or an inadvertent power supply sequencing. The forward voltage of the external Schottky diodes should be less than 500mV.

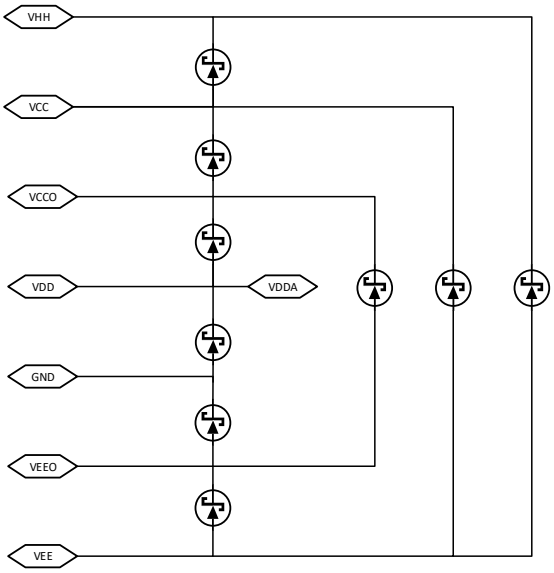

FIGURE 18: SCHOTTKY DIODES

Power Supply/Analog Voltage Sequence

Ideally, all power supplies would become active simultaneously while also meeting the power supply restrictions. However, since it is difficult to guarantee simultaneous levels, the following sequence is recommended:

1. VEE
2. VHH
3. VCC
4. VCCO
5. VDD/VDDA
6. VREF
7. VEEO

Use the reverse sequence during power down.

Chip Reset

The RESET pin is an active high input that places all internal registers to a default state. The default state for each register is shown in the register map. The internal state of the Hood registers is indeterminate following power-up and is not guaranteed on power-up alone. For this reason, a reset must be executed after a power-up to make sure all registers are in their default state. An internal pull-up resistor to VDD holds the pin high when left floating.

In addition, the SPI port can execute a reset (as a write only transaction). If the SW_RESET is written to, SW_RESET will fire off a one-shot pulse that performs the same function as an external RESET. SW_RESET is accessed in the SPI slave register using RSRC address = 14. This is shown in the register map section of the datasheet.

SPI - Host Serial Data Bus

The Hood PMU IC has a SPI Slave serial interface for host access to the Hood registers. The full digital block is shown below in **Error! Reference source not found.**.

The SPI interface consists of the following pins:

- Input serial clock (SPI_CLK)
- Data output ports (SPI_SDO_A, SPI_SDO_B)
- Data input port (SPI_SDI_A, SPI_SDI_B)
- Chip select input port (SPI_CS)

SPI_CLK, SPI_SDO_A/B and SPI_SDI_A/B can be shared among multiple Hood or other SPI Slave devices, with each device having its own dedicated SPI_CS. SPI_CS is an active low input. This is shown in Figure 19. The interface is designed to run up to 100 MHz in point-to-point configuration, with no other devices on the bus, and when all recommended PCB design guidelines are adhered to. It is the responsibility of the host device (Serial Master Device) to meet the Hood setup and hold requirements and to adjust its internal clock scheme to align the Hood read data as necessary. The clock frequency can be varied on the "fly' to allow for the slower round-trip timing on the read cycle, without sacrificing write performance and read command/address setup. Serial data is transmitted most significant bit (MSB) first. The Hood IC will latch the serial data (commands, address and write data) on the rising edge of the serial input clock. The Hood IC will by default drive read data on the falling edge of the serial input clock. Read data is by default launched 3.5 clock cycles after capturing the last address bit. The serial clock can be free running or may stop after a bus transaction.

The Hood IC requires a minimum of 32 clock cycles for a 1x bus operation, and 16 clock cycles for a 2x bus transaction. Each bus transaction must en-capsulated within an active SPI_CS pulse. The 1x and 2x bus transaction protocols are discussed below.

Respective DC and AC parameters are provided in the specification section of the datasheet.

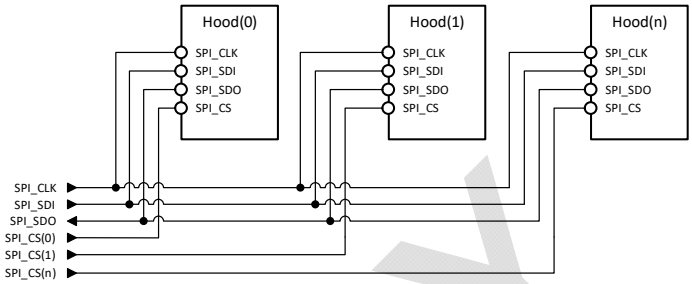

FIGURE 19: SPI INTERFACE CONNECT WITH MULTIPLE DEVICES

Host Interface Protocol

The SPI interface can be used in one of two different Bus Transaction Modes. These 2 modes are explained below:

1) Single data bit (1x) Bus Transations.

   The SPI_SDI_A and SPI_SDO_A SPI ports are used for serial data in and out.

   The serial host protocol starts with a 1-bit read/write command, followed by a 4-bit resource selection field (RSRC), followed by a 6-bit address field on SPI_SDI_A. For write commands, the address is immediately followed by a 16-bit data field, followed by 5 dummy bits. The clock cyles of the dummy bits are used to push the data into the appropriate register. During read commands immediately following the address field on SPI_SDI_A, there are 5 dummy bits after which a 16-bit data field is transmitted on the SPI_SDO_A port. Note that the Mystery IC will drive out of SPI_SDO_A on the falling edge of the serial input clock with the expectation that the host will latch each bit on the rising edge of the clock.

   If the 1x Bus Transaction protocol is used, the SPI_SDI_B pin must be grounded. The SPI_SDI_B being in a low state during the command clock phase initiates a 1x Bus Transaction.

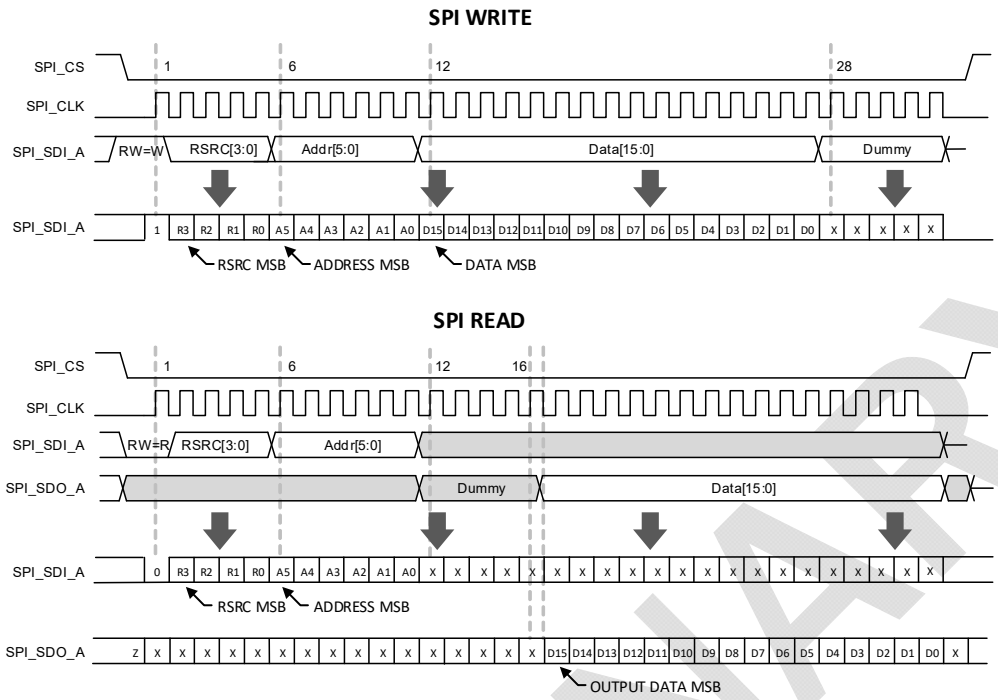

FIGURE 20: SPI INTERFACE 1X BUS TRANSACTION

2) Two data bit (2x) Bus Transactions:

The SPI_SDI_A/SPI_SDI_B and the SPI_SDO_A/SPI_SDO_B pins are used for serial data input and output. The SPI_SDI_A/SPI_SDI_B pins are used for serial input and the SPI_SDO_A/SPI_SDO_B pins are used for serial output.

The 2x bus transaction is the same as the 1x protocol except there are only 2 dummy cycles, either at the end of the data transfer for write commands or after the address phase during read commands.

The serial host protocol starts with a 1-bit read/write command on the SPI_SDI_A pin with a '1' on the SPI_SDI_B pin. This is followed by a 4-bit resource selection field (RSRC), followed by a 6-bit address field split between the SPI_SDI_A and SPI_SDI_B bits. For write commands, the address is immediately followed by a 16-bit data field split between the SPI_SDI_A and SPI_SDI_B pins, followed by 2 dummy bits on each of the input pins. The clock cyles of the dummy bits are used to push the data into the appropriate register. During read commands immediately following the address field on the SPI_SDI_A/SPI_SDI_B pins, there are 2 dummy bits after which a 16-bit data field is transmitted on the SPI_SDO_A/SPI_SDO_B ports. Note that the Mystery IC will drive out of SPI_SDO_A/SPI_SDO_B on the falling edge of the serial input clock with the expectation that the host will latch each bit on the rising edge of the clock.

The SPI_SDI_B being in a high state during the 1-bit read/write command phase initiates a 2x Bus Transaction.

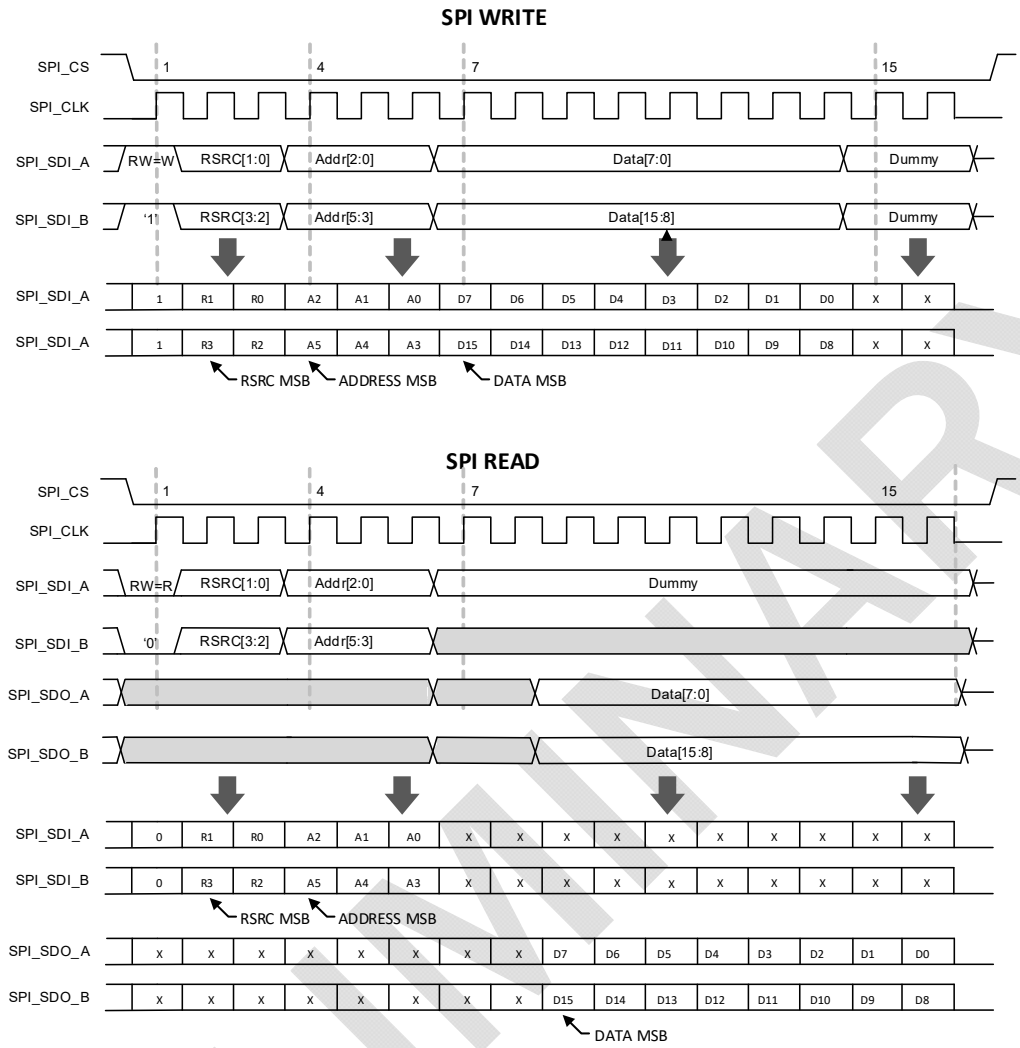

FIGURE 21: SPI INTERFACE 2X BUS TRANSACTION

- The resource field (RSRC) is a 4 bit field that selects the type of register, channel, and number of registers which will be written or read. Selecting more than one resource for reads is not valid as only one channel can be read back at once. The 4-bit resource field is decoded as shown in Table 53 below:
- To write or read any single channel register, the resource field (RSRC) is programmed to the desired channel number (0 through 7).
- RSRC value 8 - 14 are dedicated to Write-Multicast. This is writing the same value to an arbitrary combination of channels as programmed into the RSRC_REG register (addr 0xF). The RSRC_REG register default is set a '0', therefore to work as Write-Broadcast to all 8 channels, a '0xFF' must be written (which would mean that a write to any RSRC 8 – 14 will reach all 8 channels). Should another replication pattern be desired (with different channels specified), the RSRC_REG register should first be programmed with the channels desired, then issue a write to any RSRC_REG value between 8 and 14. That pattern will then stay in effect until reprogrammed, or device reset. The lower 8 bits of this RSRC_REG register are used to define multi-channel writes of any combination of channels. Bit 7 corresponds to channel 7 down to bit 0 for channel 0. Set the bit associated with the desired channels to "1" and the others to "0". For example, to multicast to all even channels you would write "01010101" (55 Hex) into the RSRC_REG register. See register description section for additional detail.
- RSRC value 15 will write the same value to all 8 channels.

TABLE 53: RESOURCE SELECTION

RSRC[3:0] Field Value (decimal)	Description
0 - 7	Remote Channel Registers
8 - 14	Write-Multicast. Use the RSRC_REG (addr 0xF) to select resource.
15	Write All Resources

Hood Digital Architecture

The digital architecture of Hood is comprised of a central control block plus 8 channel register blocks which are connected to the central block via a parallel bus.

Shadow registers

In addition to the registers roughly defined from the SPEAR chip above, all PMU resource based registers will have a shadow register defined (unique address space) to allow for simultaneous transfers between registers. Currently there are approximately 12 registers defined that will have shadow registers. A Shadow update register will be provided (resourced based, SHDW_UPD) to initiate the shadow update of the selected PMU registers. Note that if the PMU registers that are required to be shadowed is greater than 16, multiple shadow update registers will be required. The definition of the simultaneous register update is still being worked, but the basic concept is as follows:

- When a direct write access of a shadowed PMU register is written, the corresponding shadow register will be updated so the two registers will be coherent with the exact same content. The two registers will be considered in-sync.
- When a PMU shadow register is written, only the shadow register is updated with the selected fields. The direct register and the shadow register will not be coherent. The two registers will be considered out-of-sync.
- When the shadow update register is written, the contents of the selected PMU registers will be updated with the content in the shadow register. The two registers will be considered in-sync.
- PMU shadow registers can be written and read exactly like there corresponding direct access register.
- As currently defined, shadow register writes and the shadow update write needs to be an atomic operation for correct behavior. Updating only the shadow register fields that change when a direct register write occurs could minimize, but not necessarily eliminate the need for an atomic simultaneous update operation.

.

Central Registers

The central block contains the SPI serial port interface, channel register control and management, global registers and fuse memory control. The channel register control and management block in the main digital block is the interface between the SPI serial port and the channel registers in the channel register blocks. It also has global registers that control global chip functionality.

As mentioned above, the Hood IC has fuse memory onboard to hold specific calibration data. These fuses are OTP (One Time Programmable) memory; meaning non-volatile and can be written only once. This memory is written during ATE test and hold various register values used to achieve optimal performance in the device. The data that is stored in OTP is explained in this datasheet and can be programmed to be used or bypassed, but it cannot be read.

Channel Register Blocks

The central block is connected to the eight remote blocks via a parallel bus interface. All the channel register blocks contain the same set of registers for each channel. They are differentiated in addressing only by the RSRC field of SPI frame, or the RSRC_REG when Write-Multicast is used. Write-Broadcast can be used to speed up configuration, which is by concurrently setting up all channels.

Register Bit Mapping

Many registers have multiple smaller bit fields that can written independently without affecting the other bit fields in that register. For these registers each independent bit field has a WE (write enable) bit defined that must be set to "1" for those bits to be affected by a write. Any bit fields whose WE bit is set to "0" during a write to that register will not be changed. Not all register have WE bits.

DAC Implementation

Each channel has 17, 16-bit integrated DAC level registers. These 17 registers drive 9 actual DACs. Some of the DAC level registers are shared between the 9 actual DACs, with the shared implementation of this show in Table 54 below. Not all the DACs are shared.

Before using each of the DAC levels, each of the DACs need to be enabled independently of each other.

The Voltage Clamps and Current Clamps do not use a 16-bit DAC to set the clamp levels. The clamps are set in the channel registers using an 8-bit DAC. These DACs do not need to be enabled before use.

The DACs are shown below:

TABLE 54: DAC LEVEL IMPLEMENTATION

DAC	Enable Bit	Shared Levels
FI	FI_DACENA	N/A
CVA	COMP_DACENA	CVA, CVA_DIFF, CVA_PMU_MV, CVA_PMU_MI
CVB	COMP_DACENA	CVB, CVB_DIFF, CVB_PMU_MV, CVB_PMU_MI
VTT	VTT_DACENA	VTT, VTT_ILOAD
FV	FV_DACENA	FV, FV_B

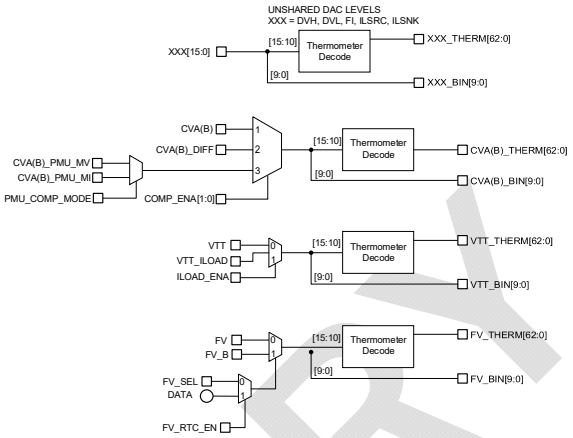

FIGURE 22. THERMOMETER DECODE BLOCK DIAGRAM

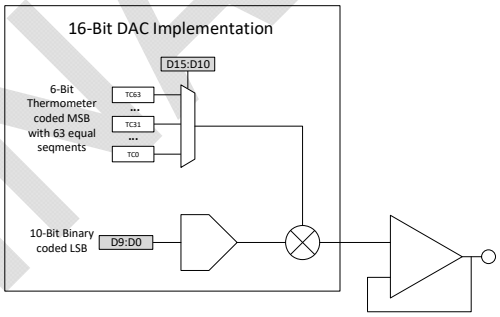

FIGURE 23: DAC ARCHITECTURE

DAC Thermometer Mode

Each channel's remote register block interfaces with the DAC's. Each DAC is implemented as 10-bit binary LSB DAC plus a 63 segment thermometer coded MSB DAC. The 10 LSB bits are passed through directly, but the 6 MSB's must be decoded to a 63-bit thermometer code value.

In this mode the 10-bit binary DAC overlaps each thermometer segment and each segment will have to be calibrated individually. This means calibrated values must be written to the DAC register.

The Diagram below shows the Thermometer decode implementation.

DAC Offset Correction

There are 13 DAC offset level correction registers that can be used to optimally center the voltage range of each DAC by shifting the range up and down. These registers change the offset of the DAC up to +/-500mV max. There is no offset associated with the Active Load.

This offset is applied digitally to the register level before being fed into the DAC.

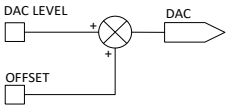

FIGURE 24: DAC OFFSET

TABLE 55: OFFSET CORRECTION RANGE

Code	VALUE
0000	-500mV
1000	0mV
1111	+500mV

DAC Offset Implementation

As seen above, many of the DACs are used for more that one mode. For example, the CVA DAC is used for single ended compare, differential compare, and PMU compare. For this reason, there are more offset registers than there are DACs. The offset register used for each DAC is based on the mode selected during usage. The shared offset registers are shown below along with the modes used for each. There is no offset associated with the active loads.

TABLE 56: DAC OFFSET REGISTERS

DAC Offset Register	When Offset Register Is Used	Modes	DAC
OS_DVH_HS[3:0]	DRV_ENA[1:0] = 0, 1, or 3	Driver HS Mode Driver Standy Mode	DVH
OS_DVH_HV[3:0]	DRV_ENA[1:0] = 2	Drive HV Mode	DVH
OS_DVL_HS[3:0]	DRV_ENA[1:0] = 0, 1, or 3	Driver HS Mode Driver Standy Mode	DVL
OS_DVL_HV[3:0]	DRV_ENA[1:0] = 2	Drive HV Mode	DVL
OS_VTT_HS[3:0]	(DRV_ENA[1:0] = 0, 1, or 3) And (ILOAD_EN = 0)	Driver HS Mode Driver Standy Mode	VTT
OS_VTT_HV[3:0]	(DRV_ENA[1:0] = 2) And (ILOAD_EN = 0)	Driver HV Mode	VTT
OS_VTT_ILOAD[3:0]	ILOAD_EN = 1	Active Load Enabled	VTT
OS_CVA[3:0]	COMP_ENA = 0, 1, or 2	Comparators Disabled Single Ended Compare Mode PPMU Compare Mode	CVA
OS_CVB[3:0]	COMP_ENA = 0, 1, or 2	Comparators Disabled Single Ended Compare Mode PPMU Compare Mode	CVA
OS_CVA_DIFF[3:0]	COMP_ENA = 3	Differential Compare Mode	CVA_DIFF
OS_CVB_DIFF[3:0]	COMP_ENA = 3	Differential Compare Mode	CVB_DIFF
OS_FI[3:0]	At all times	Force Current Mode	FI
OS_FV[3:0]	FV or FV_B	Force Voltage Mode	FV
OS_ILSRC[3:0]	N/A	Not Implemented	N/A
OS_ILSRC[3:0]	N/A	Not Implemented	N/A

Device ID and Device Rev

The Device ID and the Device Rev information is stored on-chip and can be read back using the SPI port. This information is stored in read only registers that identify the product identification and device revision.

The details of these 2 registers can be viewed in the Global Registers table using the DEV_ID and the DEV_REV registers.

Register	Description
DEV_ID	Device Identification
DEV_REV	Device Revision

Note: DEV_ID = 0?? Hex = ??? Decimal.

Register Types

TABLE 57: REGISTER TYPES

Register	Description
WO_PULSE	Write Only, one shot pulse (no storage). A write to this register will trigger an internal pulse.
WE	Write Enable (no storage)
RW	Read/Write (storage for write)
RO	Read Only (no storage, live)
ROL	Read only Latched (storage for external signal)
ROL_CLR	Read only Latched, Clear on Read (storage for external signal is reset by reading register)

Register Maps

Global Registers

Located in central digital block. Only one copy of each of these registers is in the chip.

TABLE 58: GLOBAL REGISTERS

REG_NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
GLBL_CSR	0x00	[15]	RC		**LFSR_ERR:** LFSR register detected an error	
		[14]	RC		**SPI_ERR:** SPI state machine detected an error. CS went away before enough clocks occurred to complete the bus transaction.	
		[13]	RC		**SPI_CKERR:** SPI interface received extra sck under CS. Extra clocks are ignored by SPI controller and is more of a status then an error.	
		[12:3]	-		***Reserved***	
		[2]	WE		**RB_INVERT_WE:**	
		[1]	RW		**RB_INVERT:** Invert the read back data. Used to test Channel based Memories simultaneously. Only inverts Channel based registers, except channel registers documented as not invertible.	
		[0]	W		**RST:** Global Reset (functionality currently undefined, but does not reset register fields)	
DEV_ID	0x04	[15:12]	-	-	**Reserved (unused)**	
		[11:0]	RO	-	**CHIP_ID:** Chip identification. Elevate chip ID is 'XXXh'	**DEV_ID[11:0]**
DEV_REV	0xFC	[15:12]	-	-	**Reserved (unused)**	
		[11:8]	RO	1	**MAJOR_REV:** This bit field is incremented to indicate significant changes that require modification of the software. First silicon starts at revision 0001.	**DEV_REV[11:0]**
		[7:4]	RO	1	**MINOR_REV:** This bit field is incremented to indicate minor changes that are 100% backwards compatible with software for all previous versions of the chip. This could include adding of features or bug fixes that do not have any impact on software (i.e. stay disabled or don't impact previous behavior by default). The functionality of the previous version is maintained without any changes to software. First silicon starts at revision 0001.	
		[3:0]	RO	1	**BUILD_REV:** This bit field is incremented to indicate a modification that has no impact on functionality or behavior. These changes might include those for yield enhancement, reliability improvement or parametric shifts. Changes are 100% compatible with all previous versions of software. First silicon starts at revision 0001.	
RSRC_REG	0xF0	[15:9]	-	-	***Reserved (unused):***	**RSRC_REG**

REG_NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
		[7]	RW	0	**CHANNEL_7:**	
		[6]	RW	0	**CHANNEL_6:**	
		[5]	RW	0	**CHANNEL_5:**	
		[4]	RW	0	**CHANNEL_4:**	
		[3]	RW	0	**CHANNEL_3:**	
		[2]	RW	0	**CHANNEL_2:**	
		[1]	RW	0	**CHANNEL_1:**	
		[0]	RW	0	**CHANNEL_0:**	
CALBUS_FRC	0x08	[15:11]	-	-	***Reserved (unused):***	
		[10]	WE	-	**FORCE_ENA_WE:**	
		[9]	RW	0	**FORCE_ENA:** Connects CAL_FH bus to the output pad. "0" sets output pin to HiZ.	**FORCE_ENA**
		[8]	WE	-	**FORCE_WE:**	
		[7:0]	RW	0	**FORCE:** Bit 7 Connects Channel 7 to FORCE bus. Bit 6 Connects Channel 6 to FORCE bus. .... Bit 0 Connects Channel 0 to FORCE bus.	**FORCE_OUT[7:0]**
MON_SEL_0	0x0C	[15:8]	RW	0	**MON_ML_0:** Connects channel ML bus to the appropriate MON_ML bus. Bit 7 – connect channel 7 .... Bit 0 – connect channel 0	**MON_ML_0[7:0]**
		[7:0]	RW	0	**MON_MH_0:** Connects channel MH bus to the appropriate ADC_MH bus. Bit 7 – connect channel 7 .... Bit 0 – connect channel 0	**MON_MH_0[7:0]**
MON_SEL_1	0x10	[15:8]	RW	0	**MON_ML_1:** Connects channel ML bus to the appropriate MON_ML bus. Bit 7 – connect channel 7 .... Bit 0 – connect channel 0	**MON_ML_1[7:0]**
		[7:0]	RW	0	**MON_MH_1:** Connects channel MH bus to the appropriate ADC_MH bus. Bit 7 – connect channel 7 .... Bit 0 – connect channel 0	**MON_MH_1[7:0]**
MON_XCTRL	0x14	[15:10]	-	-	***Reserved (unused):***	
		[9]	WE	-	**CALML_ENA_WE:**	
		[8]	RW	0	**CALML_ENA:** Connects CAL_ML bus to output pad. "0" sets output pad to HiZ.	**CALML_ENA**
		[7]	WE	-	**CALMH_ENA_WE:**	
		[6]	RW	0	**CALMH_ENA:** Connects CAL_MH bus to output pad. "0" sets output pad to HiZ.	**CALMH_ENA**
		[5]	WE	-	**MXH_ENA_WE:**	
		[4:3]	RW	0	**MXH_ENA:** Bit 1 - Enables connection of CAL_MH bus to MON_MH[1] bus. Bit 0 - Enables connection of CAL_MH bus to MON_MH[0] bus.	**MXH_ENA[1:0]**
		[2]	WE	-	**MXL_ENA_WE:**	
		[1:0]	RW	0	**MXL_ENA:** Bit 1 - Enables connection of CAL_ML bus to MON_ML[1] bus. Bit 0 - Enables connection of CAL_ML bus to MON_ML[0] bus.	**MXL_ENA[1:0]**
SHDW_UPD	0xE8	[15:0]	-	-	**Reserved (unused)**	
		[9]	RW	0	**SSPARE:** If set, Update the SSPARE with the contents of the SPARE shadow register	
		[8]	RW	0	**FI:** If set, Update the FI register with the contents of the FI shadow register	

REG_NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
		[7]	RW	0	**FV:** If set, Update the FV register with the contents of the FV shadow register	
		[6]	RW	0	**FV_ICLSNK:** If set, Update the FV_ICLSNK register with the contents of the FV_ICLSNK shadow register	
		[5]	RW	0	**FV_ICLSRC:** If set, Update the FV_ICLSRC register with the contents of the FV_ICLSRC shadow register	
		[4]	RW	0	**FI_VCH:** If set, Update the FI_VCH register with the contents of the FI_VCH shadow register	
		[3]	RW	0	**FI_VCL:** If set, Update the FI_VCL register with the contents of the FI_VCL shadow register	
		[2]	RW	0	**PMU_IRNG:** If set, Update the PMU_IRNG register with the contents of the PMU_IRNG shadow register	
		[1]	RW	0	**PMU_CFG:** If set, Update the PMU_CFG register with the contents of the PMU_CFG shadow register	
		[0]	RW	0	**PWRCTL:** If set, Update the PWRCTL register with the contents of the PWRCTL shadow register	
LST_XFER	0xEC	[15:0]	RW		**LST_XFER**	
LFSR	0xF4	[15:0]	RW		**DIAGNOSTIC LFSR**	
DIAG	0xF8	[15:0]	RW		**DIAGNOSTIC DATA**	

Remote Register Block Addresses

Per Channel Configuration and Miscellaneous Control. There will be 8 copies of the remote registers connected to the central digital block via a parallel bus interface

TABLE 59: REMOTE REGISTER BLOCK

REG NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
PWRCTRL	0x20	[15:6]	-	-	***Reserved (unused)***	
		[5]	WE	-	**FI_DACENA_WE:**	
		[4]	RW	0	**FI_DACENA:** Power up enable for FI level DAC. Controls "Enable DAC" pin on the FI DAC core.	**FI_DACENA**
		[3]	WE	-	**FV_DACENA_WE:**	
		[2]	RW	0	**FV_DACENA:** Power up enable for FV level DAC. Controls "Enable DAC" pin on the FV DAC core.	**FV_DACENA**
		[1]	WE	-	**PMU_ENA_WE:**	
		[0]	RW	0	**PMU_ENA:** Power up enable for PMU . 0 = Low power standby state, 1 = Enabled	**PMU_ENA**
PMU_CFG	0x24	[15:11]	-	-	***Reserved (unused)***	
		[10]	WE	-	**FB_WE:**	
		[9:8]	RW	10	**FB:** This bit selects the PMU feedback mode. 00 = Output stage feedback from amplifier output (internal side of sense resistor). 01 = Output stage internal feedback from DUT output. When PMU_CFG_FB=0b1 the pmu connect switch (PMU_CFG_CONNECT) is in the feedback path. Therefore when the pmu connect switch is opened the FB bit should be set back to 0b0. 10 = Output stage feedbck from just inside connect switch. 11 = Do not use	**FB[1:0]**
		[7]	WE	-	**LOOP_WE:**	
		[6]	RW	0	**LOOP:** This bit selects between tight loop operation and normal operation on the PMU. Tight loop is used for setting a stable default condition. 0 = Tight loop enabled (typically used when not connected) 1 = Select sense point from DUT_SENSE_SEL	**LOOP**
		[5]	WE	-	**FI_FV_WE:**	
		[4]	RW	0	**FI_FV:** This bit selects between FI or FV mode. 0 = FV 1 = FI	**FI_FV**
		[3]	WE	-	**DUTSAFE_WE:**	
		[2]	RW	0	**DUTSAFE:** Connects high impedance resistance to GND to FORCE pin.	**DUTSAFE**
		[1]	WE	-	**CONNECT_WE:**	
		[0]	RW	0	**CONNECT:** This bit enables PMU output. 0 = PMU output is tri=stated. Use this state for Measure Only mode as well as disconnect. 1 = PMU is active	**CONNECT**
PMU_IRNG	0x28	[15]	-	-	***Reserved (unused)***	
		[14]	WE	-	**PMU_GM_WE:**	

REG NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
		[13]	RW	1	**PMU_GM:** Recommended settings: 50mA Range use 0b0 2mA to 2uA range use 0b1 Higher output gm is needed for stability with 2uA and 20uA and improves settling time significantly. The power dissipation adder is acceptable for the lower current ranges but not for 50mA range.	**PMU_GM**
		[12]	WE	0	**COMPC_WE:**	
		[11:7]	RW	11000	**COMPC:** This bit selects compensation capacitor. Each bit enables one. Bit 0 = 10pF Bit 1 = 20pF Bit 2 = 40pF Bit 3 = 70pF Bit 4 = 150pF Recommended settings: For Cload ≤ 150pF use 0b11000 For Cload ≤ 0.1uF use 0b11111	**COMPC[5:0]**
		[6]	WE	-	**RNG_WE[5:0]:**	
		[5:0]	RW	00001	**RNG[5:0]:** PMU Range selection: Bit 0 = Selects PMU FI/MI range of 2uA (250 kΩ resistor) Bit 1 = Selects PMU FI/MI range of 20uA (25 kΩ resistor) Bit 2 = Selects PMU FI/MI range of 200uA (2.5 kΩ resistor) Bit 3 = Selects PMU FI/MI range of 2mA (250 Ω resistor) Bit 4 = Selects PMU FI/MI range of 15mA (33 Ω resistor). Bit 5 = Selects PMU FI/MI range of 50mA (10 Ω resistor).	**RNG[5:0]**
FI_VCL	0x2C	[15]	WE	-	**SPARE_1_WE:**	
		[14:9]	RW	0	**SPARE_1:**	**SPARE_1[5:0]**
		[8]	WE	-	**CLL_WE:**	
		[7:0]	RW	0	**CLL:** The PMU Low Voltage Clamp value. Programming values: · Code 0000000 (0x00) corresponds to -2.2V (nominal) · Code 1111111 (0x7F) corresponds to 4V (nominal) Bit[7] Unused.	**CLL[7:0]**
FI_VCH	0x30	[15]	WE	-	**SPARE_2_WE:**	
		[14:9]	RW	0	**SPARE_2:**	**SPARE_2[5:0]**
		[8]	WE	-	**CLH_WE:**	
		[7:0]	RW	FF	**CLH:** The PMU High Voltage Clamp value. Programming values: · Code 0000000 (0x00) corresponds to -0.0V (nominal) · Code 1111111 (0x7F) corresponds to +6.2V (nominal) Bit[7] Unused.	**CLH[7:0]**
FV_ICLSRC	0x34	[15]	WE	-	**ICLL_2mA _WE:**	
		[14:9]	RW	0	**ICLL_2mA:** Bits[2:0] used for 2mA curent clamp. Value for sourcing (from PMU to DUT) current clamp. Current clamp disabled using CLL_DIS bit. Bits [5:4] unused.	**ICLL_2mA[5:0]**
		[8]	WE	-	**ICL_WE:**	
		[7:0]	RW	0	**ICL:** Value for sourcing (from PMU to DUT) current clamp. Current clamp disabled using CLL_DIS bit.	**ICL[7:0]**
FV_ICLSNK	0x38	[15]	WE	-	**ICLH_2mA_WE:**	

REG NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
		[14:9]	RW	0	**ICLH_2mA:** Bits[2:0] used for 2mA curent clamp. Value for sourcing (from PMU to DUT) current clamp. Current clamp disabled using CLL_DIS bit. Bits [5:4] unused.	**ICLH_2mA [5:0]**
		[8]	WE	-	**ICH_WE:**	
		[7:0]	RW	0	**ICH:** Value for sinking (from DUT to PMU) current clamp. Current clamp disabled using CLH_DIS bit.	**ICH[7:0]**
FV	0x3C	[15:0]	RW	8000	**FV:** The PMU Force Voltage value. This remote register stores the calibrated value that is output from the DAC calibration state machine. This register should be written directly to control DAC when the calibration is not being used. 0000h = -2.2V nominal FFFFh = 6.7V nominal The register output should be inverted prior to sending to thermometer decode block.	**FV[15:0]**
FI	0x40	[15:0]	RW	8000	**FI:** The PMU Force Current value. FFFFh much higher than 50mA 7AE1h = 50mA, 2mA,200uA (nominal) 5037h = 0mA (nominal) 258C = -50mA, -2mA, -200uA (nominal) 0000h much less than -50mA, outside supported compliance range The register output should be inverted prior to sending to thermometer decode block.	**FI[15:0]**
PMU_SENSE	0x44	[15]	WE	-	**SPARE_S0_WE:**	
		[14:11]	RW	0	**SPARE_S0:**	**SPARE_S0[3:0]**
		[10]	WE	-	**SPARE_S1_WE:**	
		[9:5]	RW	0	**SPARE_S1:**	**SPARE_S1[4:0]**
		[4]	WE		**DISC_COMP_OUT_WE:**	
		[3]	RW	0	**DISC_COMP_OUT:**	**DISC_COMP_OUT**
		[2]	WE	-	**REMOTE_WE:**	
		[1:0]	RW	00	**DUT _SENSE _SEL:** 00 = Sense at this channels FORCE pin 01 = Sense at this channels SENSE pin 10 = Sense at neighbor channels FORCE pin 11 = NOT USED	**DUT_SENSE_SEL[1:0]**
PWRCTL_SHDW	0xA0	[15:0]	RW	0	**PWRCTL_SHDW:** SHDW register for PWR_CTRL	
PMU_CFG_SHDW	0xA4	[15:0]	RW	0	**PMU_CFG_SHDW:** SHDW register for PMU_CFG	
PMU_IRNG_SHDW	0xA8	[15:0]	RW	0	**PMU_IRNG_SHDW:** SHDW register for PMU_IRNG	
FI_VCL_SHDW	0xAC	[15:0]	RW	0	**FI_VCL_SHDW**: SHDW register for FI_VCL	
FI_VCH_SHDW	0xB0	[15:0]	RW	0	**FI_VCH_SHDW**: SHDW register for FI_VCH	
FV_ICLSRC_SHDW	0xB4	[15:0]	RW	0	**FV_ICL_SHDW**: SHDW register for FV_ICL	
FV_ICLSNK_SHDW	0xB8	[15:0]	RW	0	**FV_ICL_SHDW**: SHDW register for FV_ICL	
FV_SHDW	0xBC	[15:0]	RW	0	**FV_SHD**W: SHDW register for FV	
FI_SHDW	0xC0	[15:0]	RW	0	**FI_SHDW:** SHDW register for FI	
PMU_SENSE_SHDW	0xC4	[15:0]	RW	0	**PMU_SENSE_SHDW:** SHDW register for PMU_SENSE	
DAC_OS	0x60	[15:13]	-	-	***Reserved (unused):***	
		[12]	WE	-	**DACMODE_WE:**	
		[11]	RW	0	**FI_MODE:** Set to "1" to enable DAC binary mode operation. Default is thermometer coded operation.	**FI_MODE**
		[10]	RW	0	**FV_MODE:** Set to "1" to enable DAC binary mode operation. Default is thermometer coded operation.	**FV_MODE**
		[9]	WE	-	**OS_FI_WE:**	

REG NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
		[8:5]	RW	1000	**OS_FI:** DAC analog offset control for FI DAC. This is for adjusting the level shift offset current output from the DAC core.	**OS_FI[3:0]**
		[4]	WE	-	**OS_FV_WE:**	
		[3:0]	RW	1000	**OS_FV:** DAC analog offset control for FV DAC. This is for adjusting the level shift offset current output from the DAC core.	**OS_FV[3:0]**
MON_CTRL	0x64	[15]	WE	-	**SPARE_4_WE:**	
		[14:12]	RW	0	**SPARE_4:**	**SPARE_4[2:0]**
		[11]	WE	-	**MH_SEL_WE:**	**MH_SEL_WE**
		[10:6]	RW	0	**MH_SEL:** Selects internal channel node within the selected subgroup for connection to the channel MH(measure high) bus. 0 = No connection 1 to 31 = See Table	**MH_SEL[4:0]**
		[5]	WE	-	**ML_SEL_WE:**	**ML_SEL_WE**
		[4:0]	RW	0	**ML_SEL:** Selects internal channel node within the selected subgroup for connection to the channel ML(measure high) bus. 0 = No connection 1 to 31 = See Table	**ML_SEL[4:0]**
PMU_MISC	0x68	[15:13]	-	-	***Reserved (unused):***	
		[12]	WE	-	**CON_COMP_RSEN_WE:**	
		[11:10]	RW	11	**CON_COMP_RSEN:** This bit is used to connect compensation capacitors across Rsense. The recommended setting is to have this register bit set to 0b11 for all pmu configurations.	**CON_COMP_RSEN[1:0]**
		[9]	WE		**PMU_TESTMODE_WE:**	
		[8:6]	RW	0	**PMU_TESTMODE:** Test control bits to select internal DAC voltages to be connected to the PMU output for production test. Must also select option TBD in ADC mux control table. 0 = FV DAC 1 = FI DAC 2 = VCLH DAC 3 = VCLL DAC 4 = DUT_MUX 5-7 - unused	**PMU_TESTMODE[2:0]**
		[5]	WE	-	**ICL_METHOD_WE:**	
		[4]	RW	0	**ICL_METHOD:** This bit selects current clamp sense point	**ICL_METHOD**
		[3]	WE	-	**ICL_HYST_WE:**	
		[2:0]	RW	0	**ICL_HYST:** These bits control current clamp hysteresis. bit 2 = MSB bit 1 = inverted bit 0 = LSB 010 = min 000 = nom 101 = max	**ICL_HYST[2:0]**
PMU_DEBUG	0x6C	[15]	WE	-	**SPARE_6_WE:**	
		[14:11]	RW	0	**SPARE_6:**	**SPARE_6[3:0]**
		[10]	WE	-	**SPARE_7_WE:**	
		[9:7]	RW	0	**SPARE_7:**	**SPARE_7[2:0]**
		[6]	WE	-	**PMU_GAIN_WE:**	
		[5:4]	RW	0	**PMU_GAIN:** Selects gm settings for PMU amplifiers bit [1] = selects lower input gm bit [0] = selects lower clamp gm	**PMU_GAIN[1:0]**
		[3]	WE	-	**CLL_DIS_WE:**	
		[2]	RW	0	**CLL_DIS:** Set to "1" to disable the low clamps. This bit disables both the	**CLL_DIS**

REG NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
					current clamp and the voltage clamp.	
		[1]	WE	-	**CLH_DIS_WE:**	
		[0]	RW	0	**CLH_DIS:** Set to "1" to disable the high clamps. This bit disables both the current clamp and the voltage clamp.	**CLH_DIS**

Manufacturing

Moisture Sensitivity

The Hood is a Level 3 (JEDEC Standard 033A) moisture sensistive part. All pre-production and production shipments will undergo the following process post final test:

- Baked @+125°C ±5°C for a duration of ≥ 16 hours
- Vacuum sealed in a moisture barrier bag (MBB) within 30 minutes after being removed from the oven.

PCB Assembly

The floor life is the time from the opening of the MBB to when the unit is soldered onto the PCB.

- Product Floor Life ≤168 Hours

Units that exceed this floor life must be baked before being soldered to the PCB.

Solder Profile

The recommended solder profile is dependent upon whether the PCB assembly process is load-free.

TABLE 60: SOLDER PROFILE

Solder Profile	Pb-Free Assembly
Average ramp up rate (TL to TP)	3°C/sec (max)
Preheat • Min Temp (Ts min) • Max Temp (Ts max) • Time (min to max)(ts)	150°C 200°C 60 – 180 sec
Ts max to TL • Ramp Up Rate	3°C/sec (max)
Time above • Temperature (TL) • Time (tL)	217°C 60 – 150 sec
Peak Temperature (TP)	260°C
Time within 5°C of actual peak temp (tp)	20 sec – 40 sec
Ramp down rate	6°C/sec (max)
Time 25°C to peak temperature	8 minutes (max)

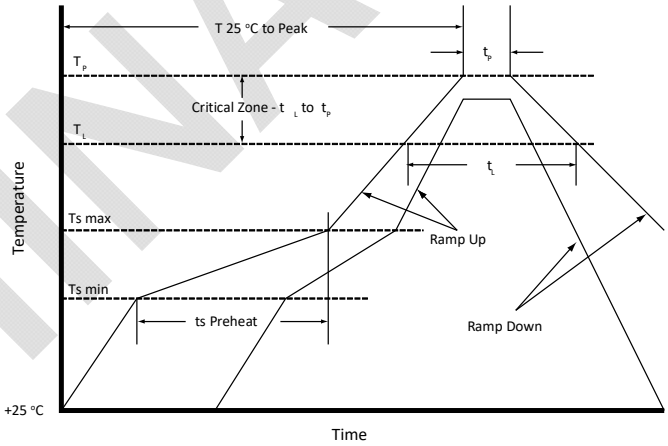

FIGURE 25: SOLDER TIME VS TEMPERATURE

Package Outline Drawing

88-Lead MLF (10mm X 10mm) with Bottom Exposed Pad

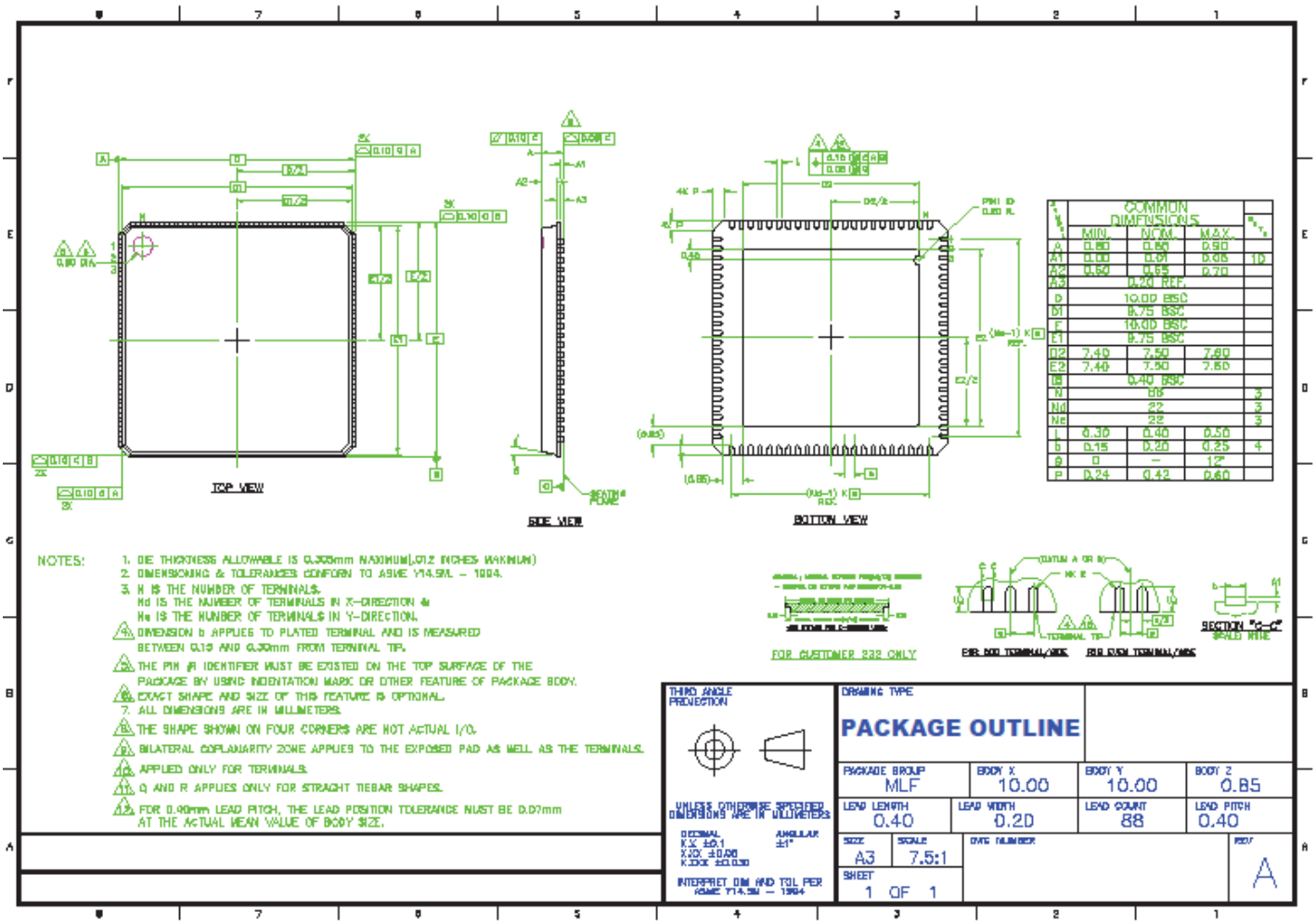

FIGURE 26: PACKAGE OUTLINE DRAWING

TABLE 61: PART NUMBER/PART MARKING

PART NUMBER (NOTE 1)	PART MARKING	TEMP RANGE (°C)	PACKAGE
TBD	TBD	+25 to +100	88 Pin, 10x10mm MLF w/bottomexposed pad

NOTE:

1. These Elevate Semiconductor Pb-free plastic packaged products employ special Pb-free material sets), molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Elevate Semiconductor Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.