Digital Inputs Single Ended Configuration

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1 Introduction

This document describes some possible methods on how to configure the differential inputs for a single-ended application.

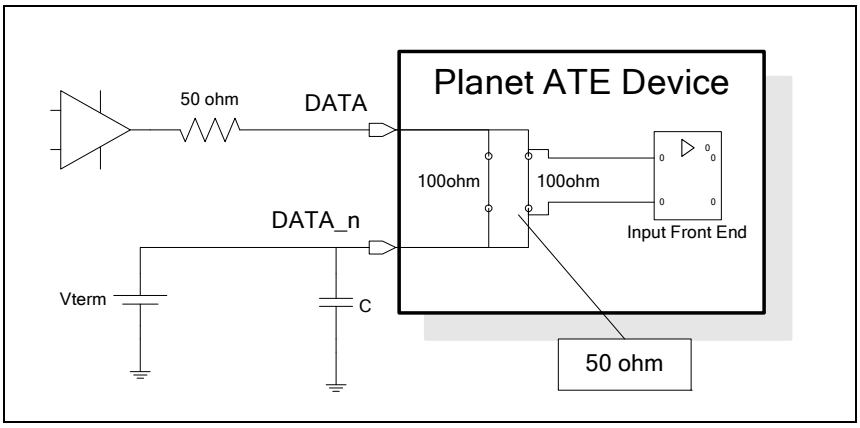
1.1 DATA and EN Inputs

Figure 1 illustrates a possible configuration for the DATA and EN inputs.

The Vterm is typically set to the external driver mid level to create a balanced symmetric swing.

The capacitor (C) should be placed close to the inverting input. The capacitor needs to handle any dynamic current response. A 0.1uF should be adequate for most applications.

Figure 1: DATA/EN Inputs



1.2 PLL_CK Inputs

The PLL_CK input could be configured as shown in Figure 1 (DATA/EN Inputs). However multiple PLL_CK inputs could be driven from a single external clock driver.

Figure 2 illustrates a possible configuration for connecting several PLL_CK inputs together.

The 50 ohm parallel termination should be placed near the last device in the serial chain. It is recommended to use an external 50 ohm resistor rather than using Device #N internal PLL Term to prevent a single board point of failure. In addition, this should simplify software configuration since it is not necessary to program the last device first. The PLL_CK signal should be routed in a daisy chain fashion; avoid long stubs to minimize reflections and transmission line effects.

The Vterm is typically set to the external driver mid level to create a balanced symmetric swing.

The capacitor (C) should be placed close to the inverting input. The capacitor needs to handle any dynamic current response. A 0.1uF should be adequate for most applications.

Figure 2: PLL_CK Inputs