ISL55180 Ganged DPS Application Note

Rev A01: 06/15/2012

This document contains information on a product under development. The parametric information contains target parameters that are subject to change.

Document Revision History

Revision	Date	Description
A01	04/30/2012	Initial Draft

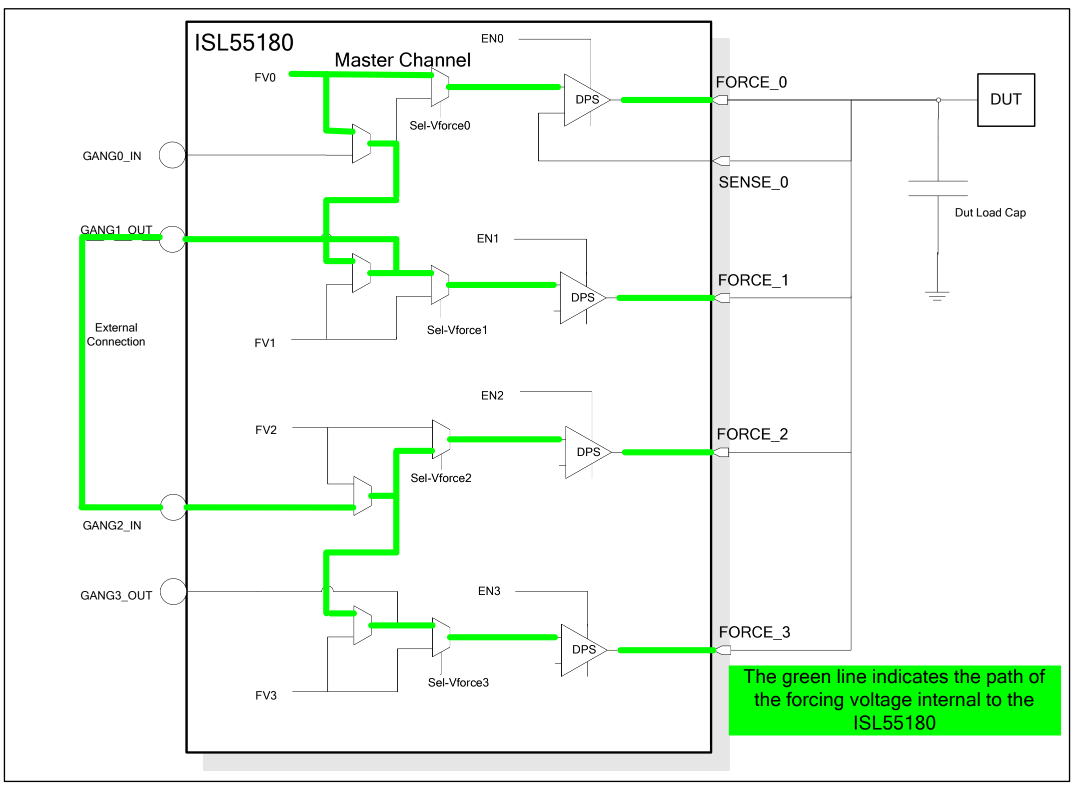
Table of Contents

Table of Figures

1 Introduction

When designing a device under test (DUT) power supply solution for Automated Test Equipment (ATE) instruments, it is preferable to design one supply channel that can satisfy the unique demands of multiple applications and DUT types so that the instrument can be leveraged across multiple end applications. One concept that is regularly employed to optimize a DPS instrument for specific DUT current requirements is to combine DPS channels to increase per channel current through a method called "ganging". There are a few common methods for ganging DPS channels and increasing current capability, each with their own trade-offs. This application note describes how to use the ISL55180 Octal Channel Integrated DPS device in a ganged application. The ISL55180 features a unique ganging architecture that makes it easy to gang DPS channels without compromising current accuracy, loop stability or transient response, with no limitations on how many channels can be ganged. When using the ISL55180, ganging is required when more than the 256mA of current per channel is required. This document focuses exclusively on the ISL55180 device. The same concept cannot be applied to our other ATE DPS products as they lack the specialized architecture of the ISL55180. Figure 1 illustrates an example of the ganged application configuration. This example does not include all muxes and switches, but just shows a high level conceptual view of 4 DPS channels ganged together to form a single 1024mA channel. In this example, channel 0 is the master channel and channels 1-3 are the slave channels. For a more detailed drawing of the ISL55180, please refer to the ISL55180 Data Sheet.

Figure 1: ISL55180 Gang Configuration Example.



Some of the main obstacles/concerns to overcome when ganging channels are:

- DPS Transient Current Response across wide current load variations
- DPS Channel Stability
- MI (Measure Current) speed vs. MI accuracy.
- Performing fine MI measurements on a ganged channel (i.e. when DUT goes into a Sleep or Stand-by mode)

1.1 Gang Mode Setup

In gang mode, all channels are configured in FV (force voltage) mode. There is one device that acts as the master and all other devices are the slaves, which follow the voltage that is programmed to the master. All FORCE_# outputs of the device which are being used in the gang mode operation are connected externally to the DUT with only the sense line of the master device connected. The sense does not have to be connected externally, but this will give the user the best overall Kelvin connection. The sequence below can be used to create a high current, ganged DPS. Note: In gang mode, the slave channel resistor/capacitor compensation network does not have any effect on the overall performance.

1.1.1 Reset the ISL55180 using either the internal CPU-Reset register or the external RESET pin. (Reset places all internal registers into a low state, but does not affect the DAC level memory).

1.1.2 Select which DPS channel will be the master channel and set the Force Voltage Level of that channel to 0V.

1.1.3 Set desired resistor/capacitor compensation on the Master Channel.

1.1.4 Set SENSE_# pin as feedback (feedback is not actually connected until channel is enabled)

1.1.5 Set Current Range.

1.1.6 Set FV-Mode (If using 256mA range, FV-Mode must be set to 0).

1.1.7 For fastest dynamic response, set Bbias#=1.

1.1.8 Set Sel-VForce#=0 of master channel

1.1.9 Set Sel-G#-Out=0 of master channel

1.1.10 Set Sel-G#-Out = 1 for all Slave Channels

1.1.11 Set Sel-VForce# = 1 for all Slave Channels

1.1.12 When ganging from an odd numbered channel to an even numbered channel, an external connection needs to be made from the GANG#_OUT pin to GANG#_IN pin.

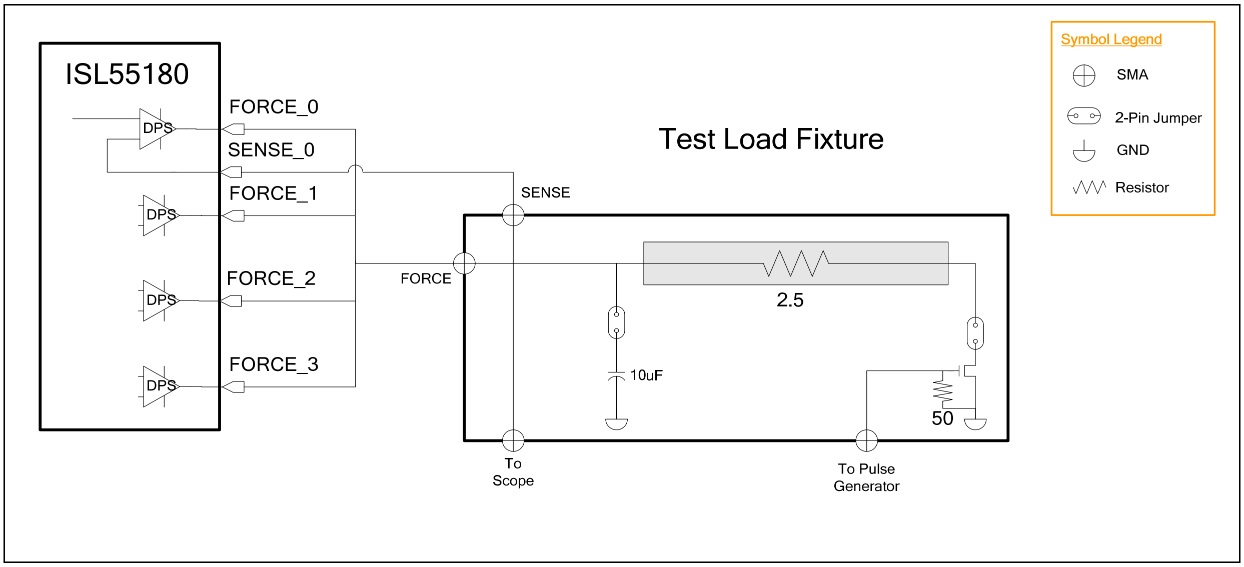
1.1.13 Enable all channels used. (Either use external EN pin or the per channel CPU-En# register. If using EN pin, SEL-RT-EN# must be set to '1').

1.1.14 Set Master channel voltage value to desired level. All slave channels will follow this voltage.

1.2 Large Current Transient Regulation

One of the main concerns of a DPS is its ability to react to a large dynamic change in loads.
Below is the output from an experiment in which there is a large output load change on the FORCE_# output with 4 channels ganged. The results from this dynamic load regulation test are shown with the test fixture included in Figure 2.

Figure 2: Large Load Change Test Circuit



The application conditions are:

- 4 Channels: 1 Master Channel (Chan 0) + 3 Slave Channels (Chan 1, 2, and 3). All within same chip.
- FV = 2.5V (8V Range)
- FV-Mode = 0
- Current Range = 256mA (IR5)
- Load Resistance = 2.5 Ω (2.5V/2.5Ω = 1A)
- Load Capacitance = 10uF
- Internal resistive compensation: Con-Res<3> connected.
- No external or internal capacitive compensation is connected.
- An external pulse generator is connected to a switch which connects or disconnects a 2.5 Ω load to ground. 50 Ω resistor is used to terminate pulse generator.

Results: Below are the results of the experiment. The measure current from the 4 ganged channels are shown.

Figure 3: 2.5V Force Voltage when changing load from 0A to 1A

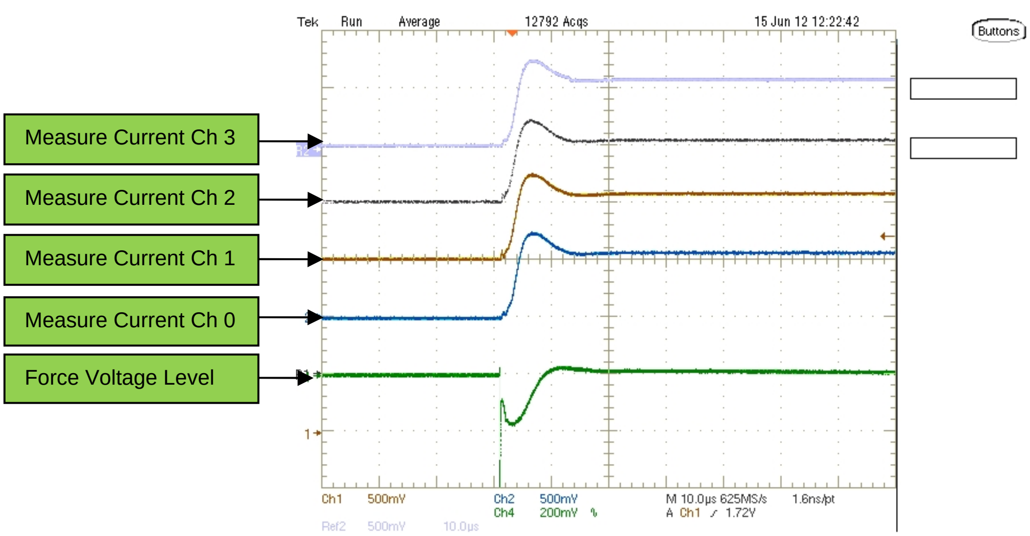
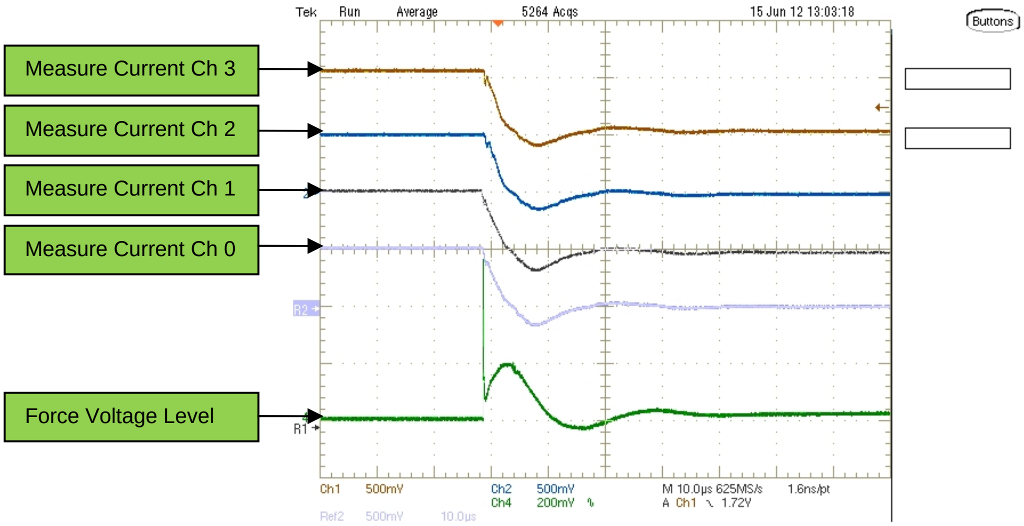


Figure 4: 2.5V Force Output Voltage when changing load from 1A to 0A



1.3 Measure Current (MI)

There are several methods to measure current in a ganged application. Three methods will be discussed in this note, although other options may be possible.

1.3.1 MI Option 1 (High Accuracy): The current from each channel used in the ganged application is measured and all currents are added together to form the total ganged current. All ganged channels are calibrated separately as a single channel for measure current and CME (common mode error). For more information on the MI calibration procedure, please see Appendix A of the ISL55180 datasheet. This method requires no additional calibration for gang mode versus single channel mode, but takes the most time.

MI(ganged) = MI(Ch0) + MI(Ch1) + MI(Ch2) + … MI(ChN): N=Number of channels ganged – 1.

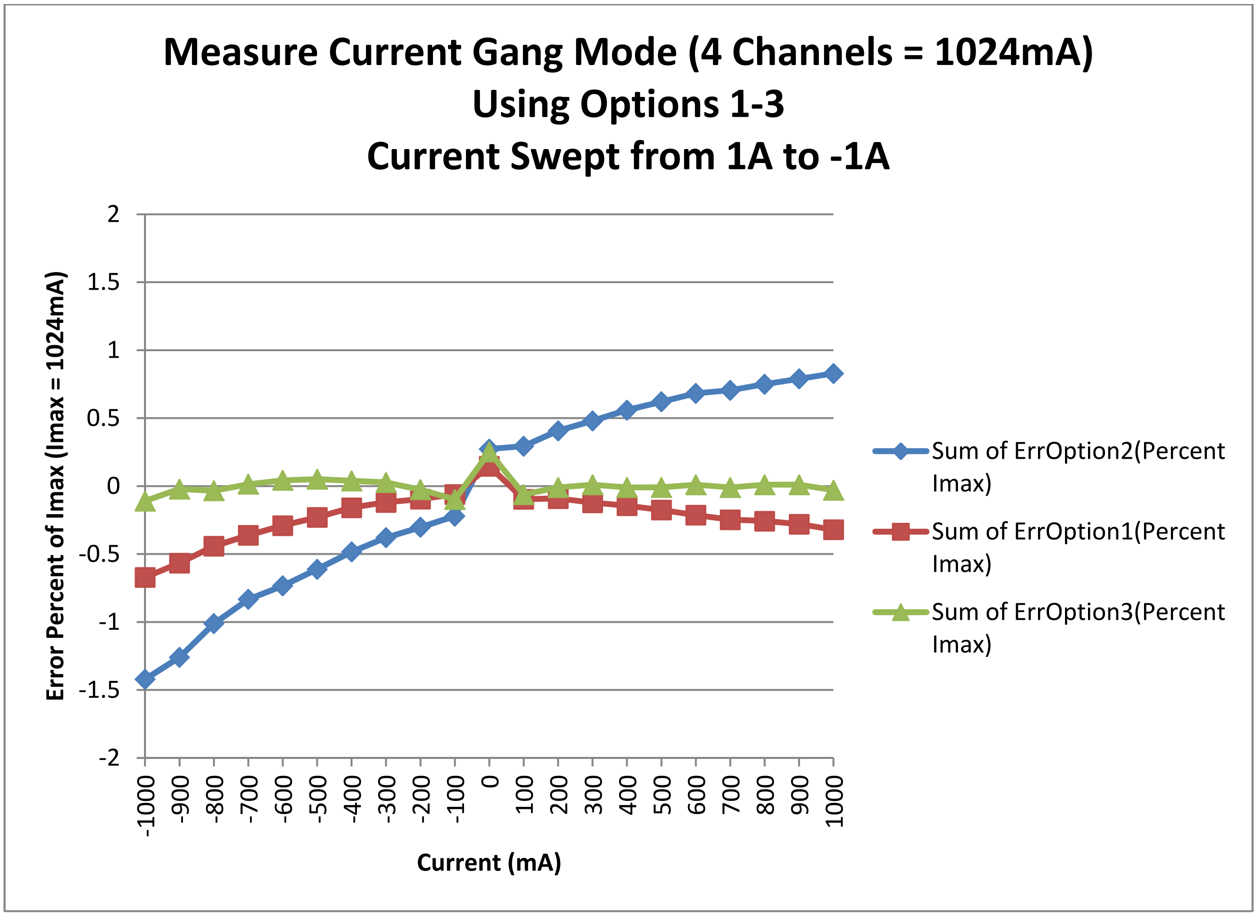
1.3.2 MI Option 2 (High Through-put): Take one MI measurement for the master channel measure and multiply the current by the number of channels used in gang mode. This method uses the calibration values from the single channel calibration and requires no additional calibration. This is the least accurate measurement technique, but is the fastest and easiest way to measure.

MI(ganged) = MI (Master) * N: N=Number of channels ganged.

1.3.3 MI Option 3 (Highest Accuracy): Calculate ganged current calibration values based on the master channel. This method requires separate calibration values for a single channel MI measurement versus a ganged channel MI measurement. With this method, a calibration value will have to be calculated based on how many channels are ganged together. In the example shown in Figure 5, a 2-segment calibration method is used. The calibration points are +25% and +75% of Full-Scale for segment 1 and -25% and -75% of Full-Scale for segment 2. Full-Scale = 1024mA.

MI(ganged) = MI(Master) * MI_ganged_gain + MI_ganged_offset

Figure 5: MI Error Using Option 1, 2, and 3



1.4 Ganging Layout

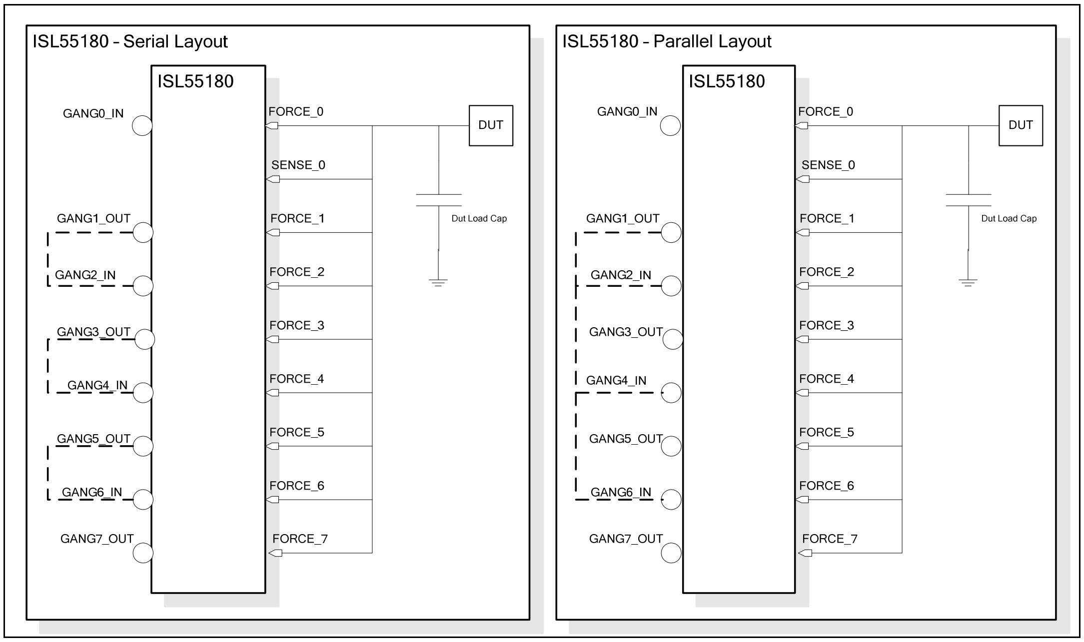
When ganging channels across multiple parts, care must be taken to choose a scheme that maximizes the performance of the ISL55180. To drive the GANG#_IN pins associated with the ganged slave channels, the main amplifier of the forcing channel is buffered by an amplifier prior to forcing a voltage on the GANG#_OUT pins. This internal amplifier helps to drive the loads associated with long trace lengths, relays, GANG#_IN pins, etc.

Figure 6 below shows 2 layout techniques which will be briefly discussed below.

1.4.1 Parallel Layout: In a parallel layout, the user will want to take the GANG#_OUT pin from the master channel and drive as many GANG#_IN pins in parallel, as possible. The parallel design method ensures the best dynamic performance is obtained. Although the parallel method is preferred, as more channels are added, the capacitance of each channel becomes visible to be buffer amplifier within the GANG#OUT pin.

1.4.2 Serial Scheme: In the serial scheme, each channel is daisy chained from one channel to the next in an order to connect all ganged channels together. Due to the daisy chaining of the channels, there is a performance lag due to the accumulation of propagation delay.

Figure 6: Serial Vs Parallel Layout



1.5 Fine Current Measurements

Many applications require the DPS to make small current measurements on the DUT; for example when the DUT goes into Sleep or Power-Down mode. In order to make precise small current measurements, the slave devices should be disabled and the master should be configured into a smaller current range. The MI current range selected depends upon the magnitude of the current being measured in the application.

This example assumes the Master is on Channel #0 and the slaves are on Channel 1 – N.

Code example for making measurements in small current range:

```
/*
       * Disconnect Slaves
       * Make measurement
       * Reconnect Slaves
       */
      for ( ch = 1 ; ch <= num_slaves ; ch++ )
      {
            /* Disable all slave channels */
            /* Could be written in parallel to all slave channels */
            V100_write_bits(DevNumber, ch, EUROPA_BIT_SEL_DPS_EN, 0);
      }

      /* Switch IR range and do MI measurement */
      V100_write_bits(dev, chan, EUROPA_BIT_IR, EUROPA_IR_25p6UA);
      current = V100_meas_pmu_mi(DevNumber, V100_CHAN0, fv, 0);
      V100_write_bits(dev, chan, EUROPA_BIT_IR, EUROPA_IR_256MA);
```



```
/*
 * Reconnect Slaves
 */
for ( ch = 1 ; ch <= num_slaves ; ch++ )
{
      /* Enable all channels */
      /* Could be written in parallel to all slave channels */
      V100_write_bits(DevNumber, ch, EUROPA_BIT_SEL_DPS_EN, 0);
}
```